

Poseidon

Schematics Document

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Poseidon 860M

Rev
-1

Date: Tuesday, June 17, 2014

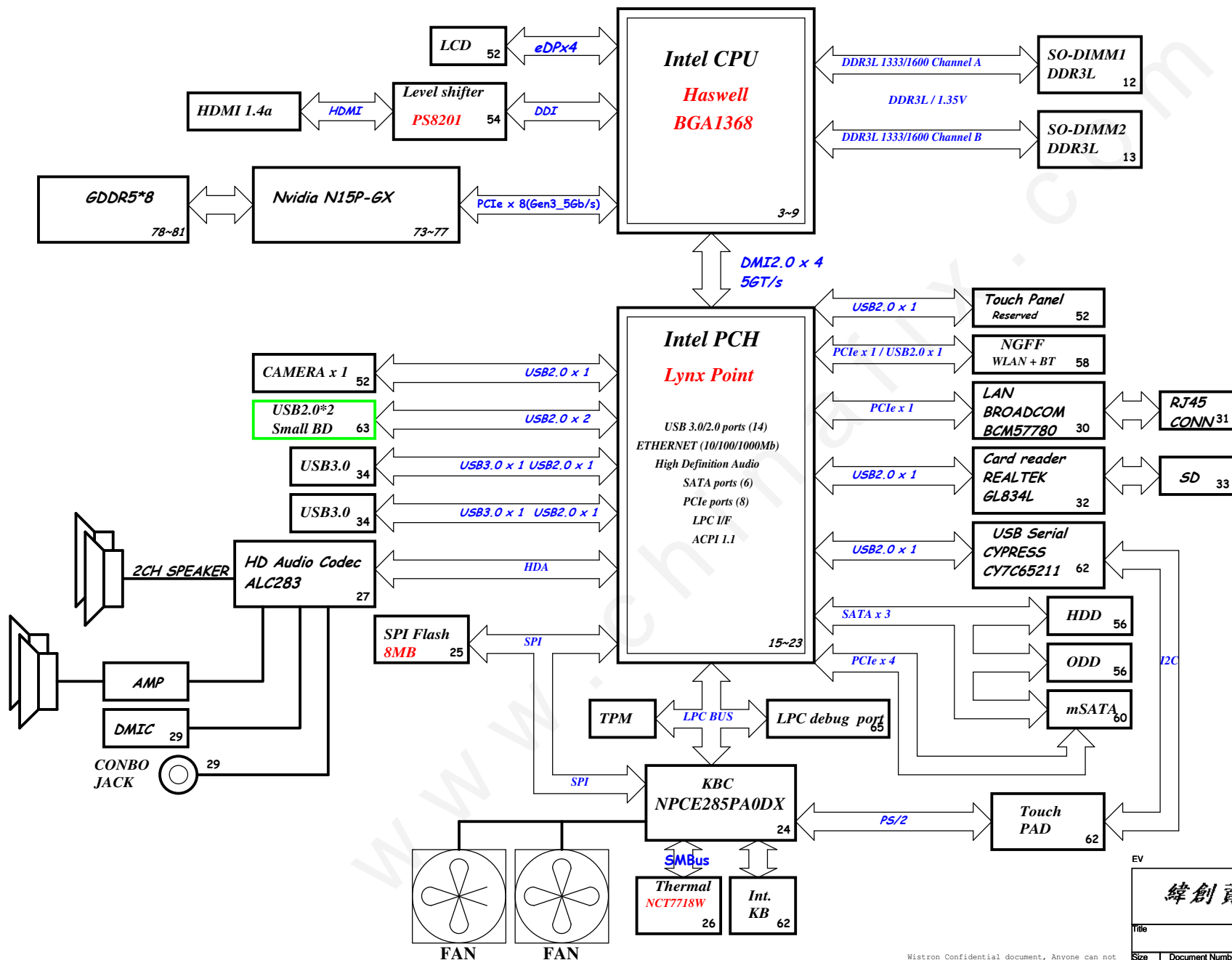
Sheet 1 of 102

Poseidon Board Block Diagram

Project code : 4PD02G010001

PCB NO : 14203

Revision : -2



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Title Block Diagram	
Size Custom	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Sheet 2 of 102
Rev -1	

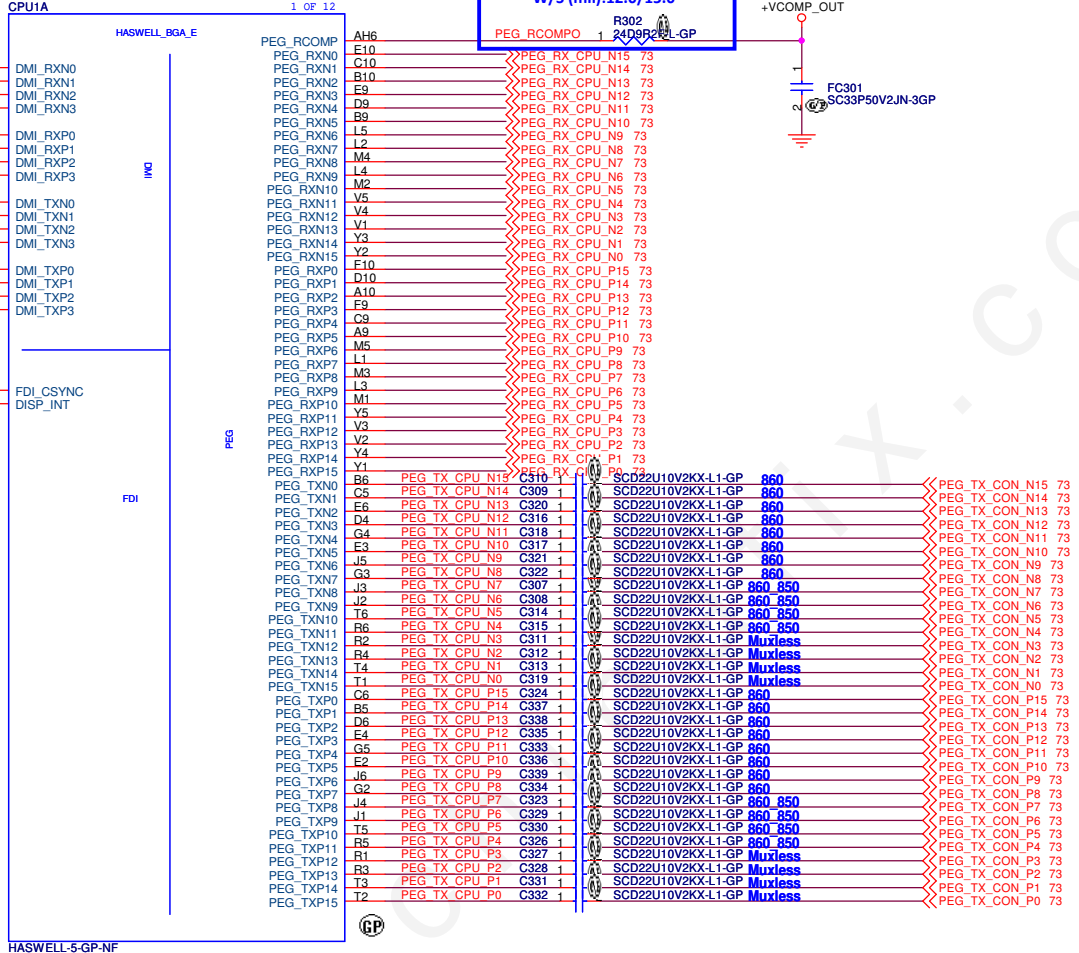
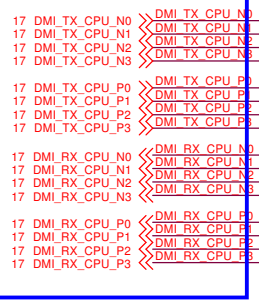
SSID = CPU

Layout Note:

Max Length : 400 Mil
W/S (mil):12.0/15.0

Max Length : 1000~8000 Mil
Max Via : 3

Layout Note:



71.HASWE.D0U

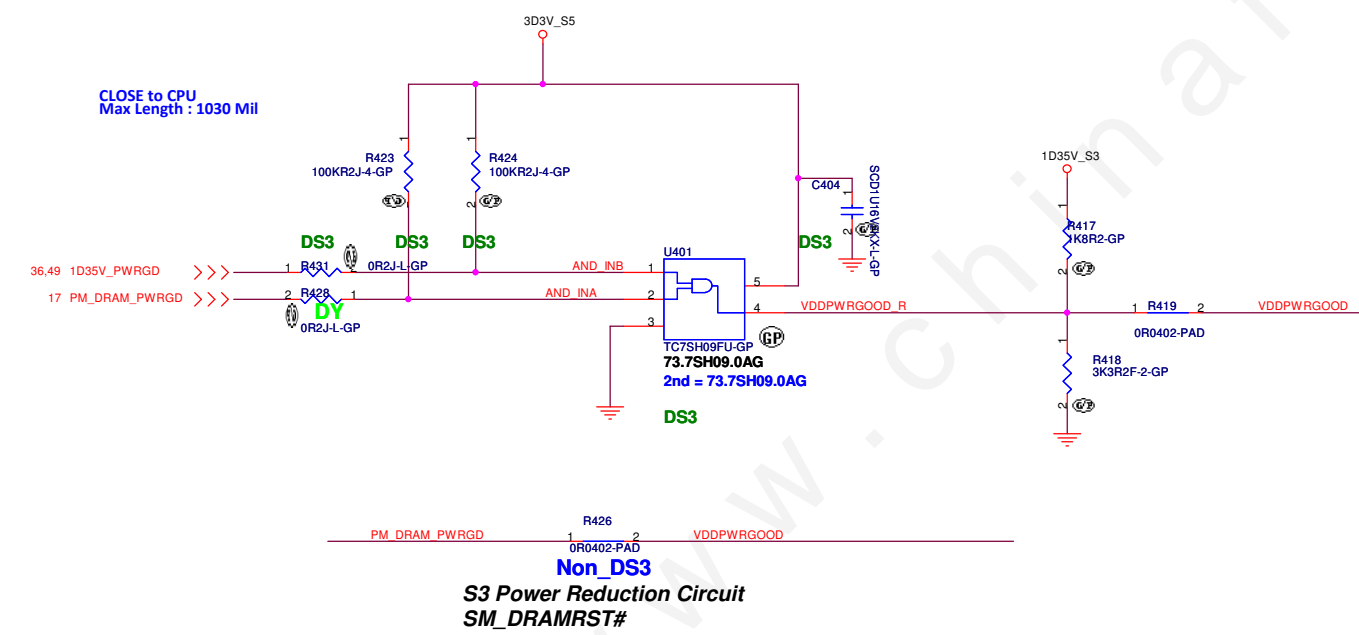
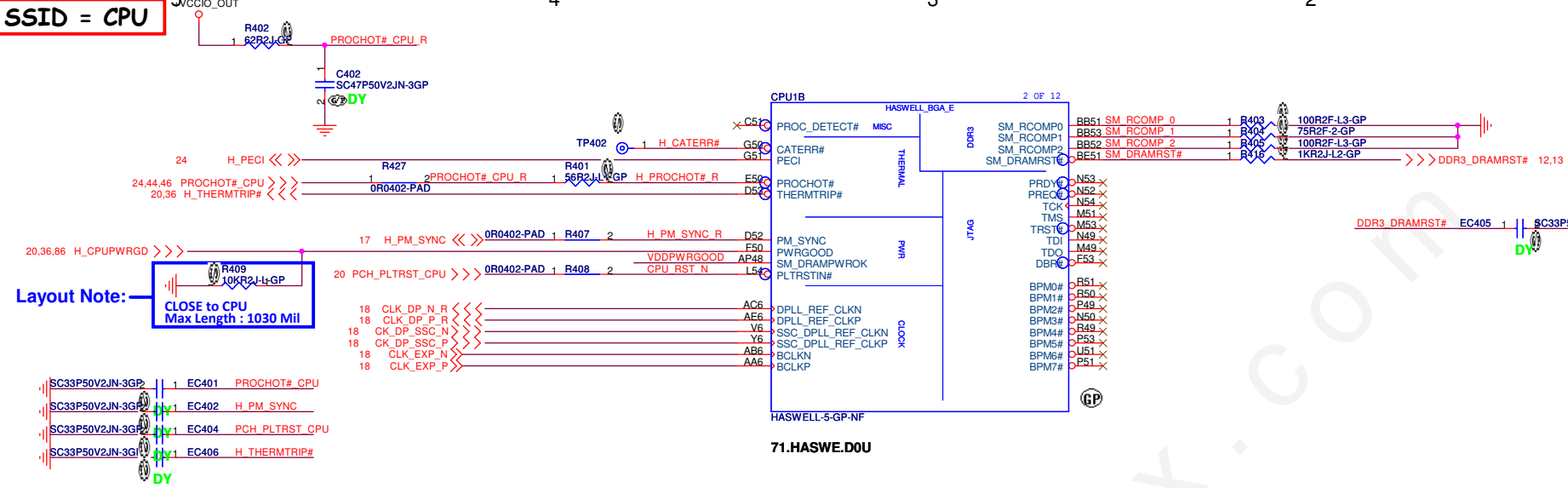
x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	1	1	1	1	1	1	2	2	7	6	5	4	3	2
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

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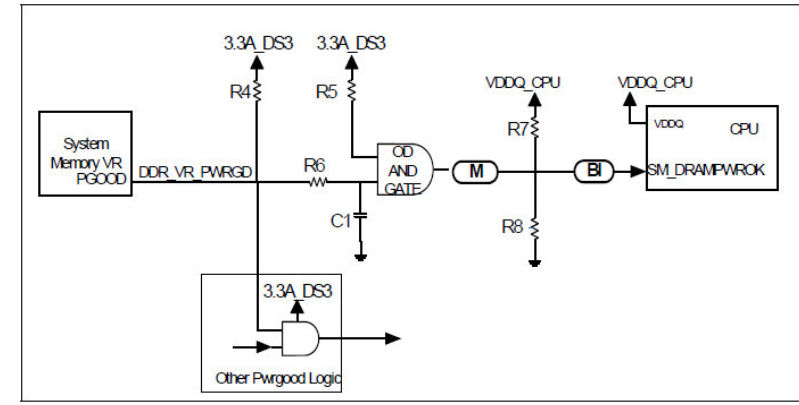
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: CPU (PCIe/DMI/FDI)</p>		
Size A3	Document Number	Rev
	Poseidon 860M	-1
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SSID = CPU



SM_DRAMPWROK Topology for platforms supporting Deep S3

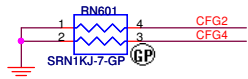


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SSID = CPU

PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed

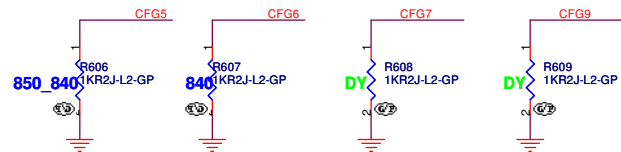


eDP Enable

CFG4 1: Disable
0: Enable

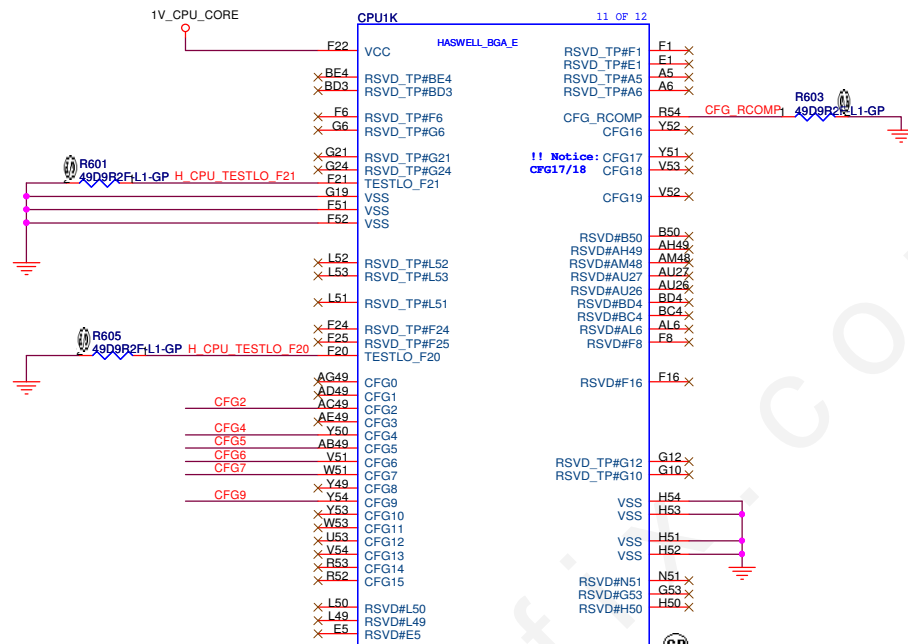
PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

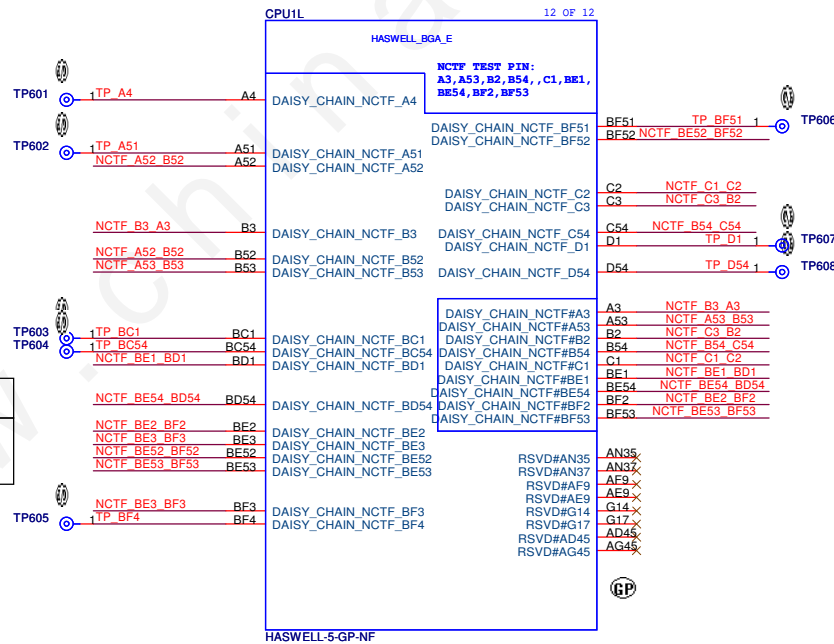


Reserved configuration lanes. A test point may be placed on the board for these lands.

CFG[19:7]



HASWELL-5-GP-NF
71.HASWE.D0U



HASWELL-5-GP-NF
71.HASWE.D0U



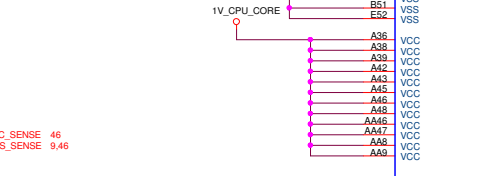
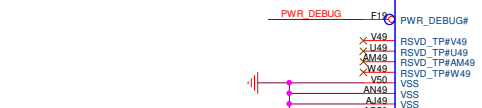
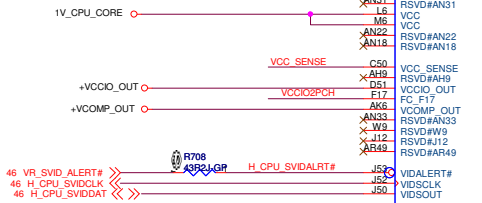
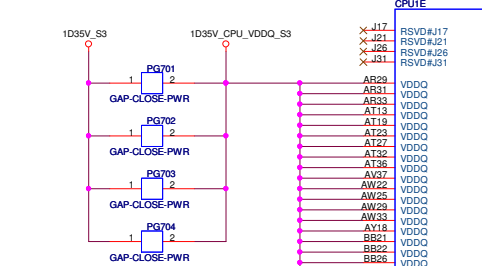
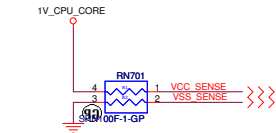
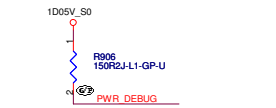
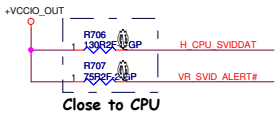
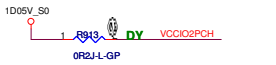
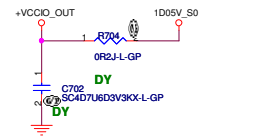
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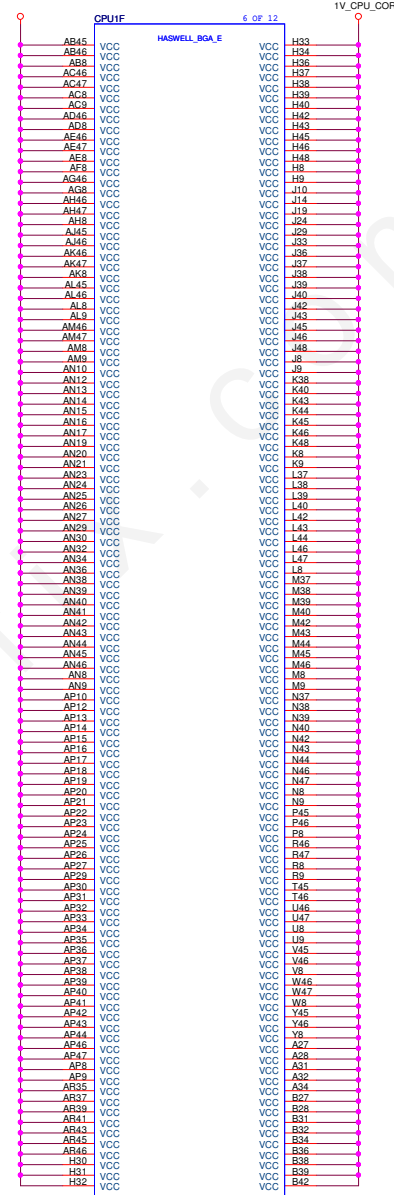
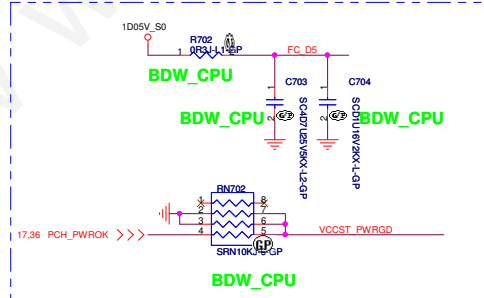
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Title		
CPU (CFG)		
Size	Document Number	Rev
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SSID = CPU



71.HASWE.D0U



71.HASWE.D0U

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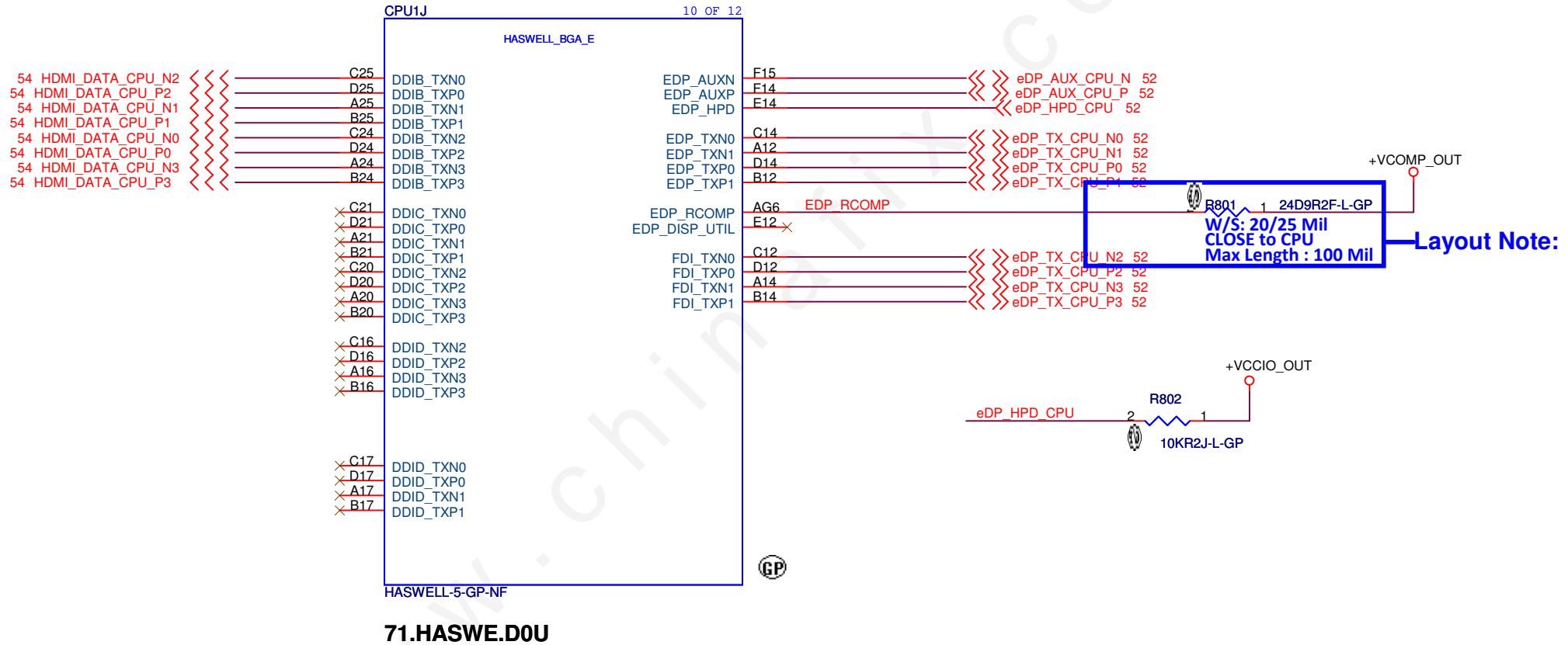
Title CPU (VCC CORE)
Size Document Number Poseidon 860M
Date: 1080509, June 17, 2014 Sheet 7 of 102

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SSID = CPU



HDMI



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Title

CPU (DDI/EDP)

Size
A4

Document Number

Poseidon 860M

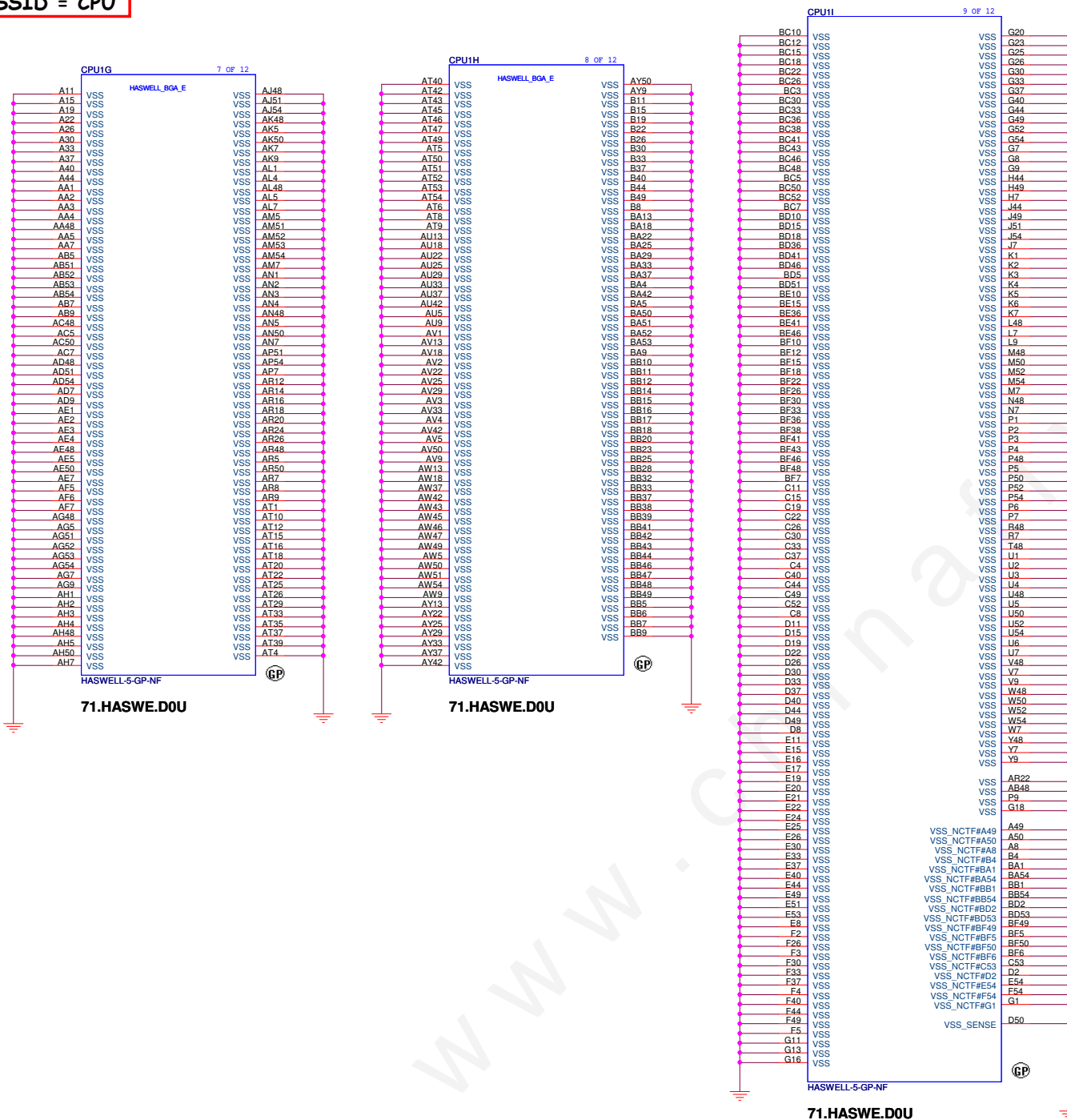
Rev
-1

Date: Tuesday, June 17, 2014

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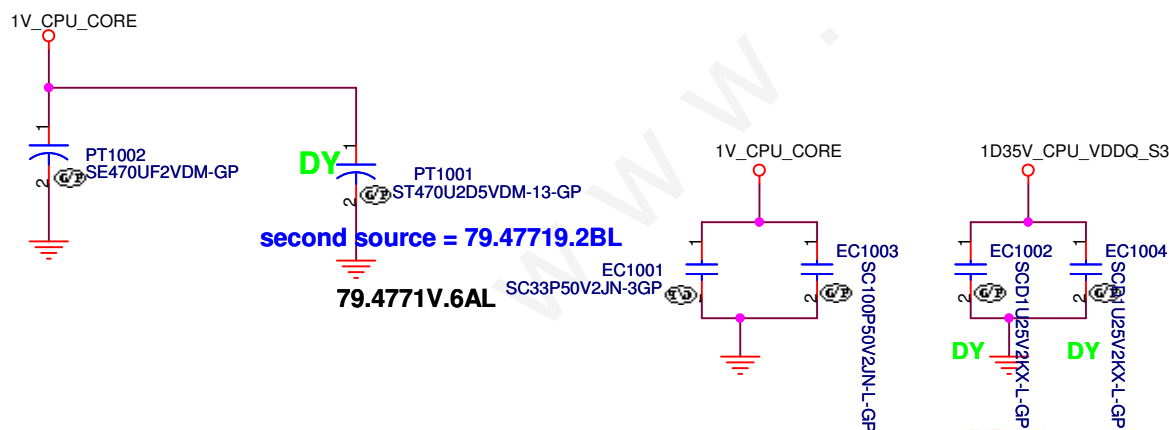
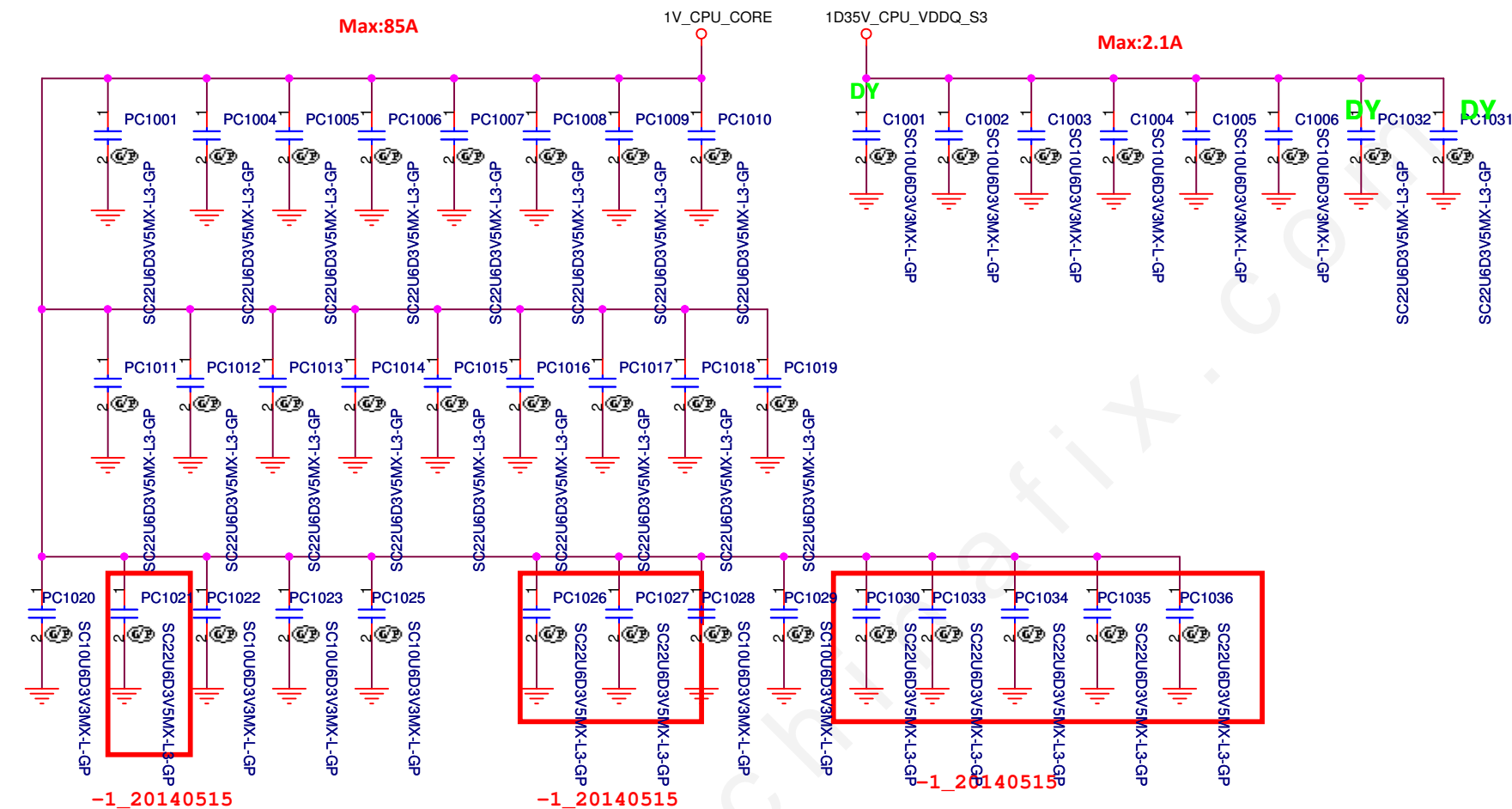
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SSID = CPU



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Title		
CPU (VSS)		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date	Tuesday, June 17, 2014	Sheet 9 of 102

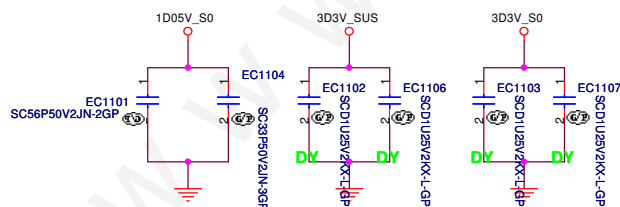
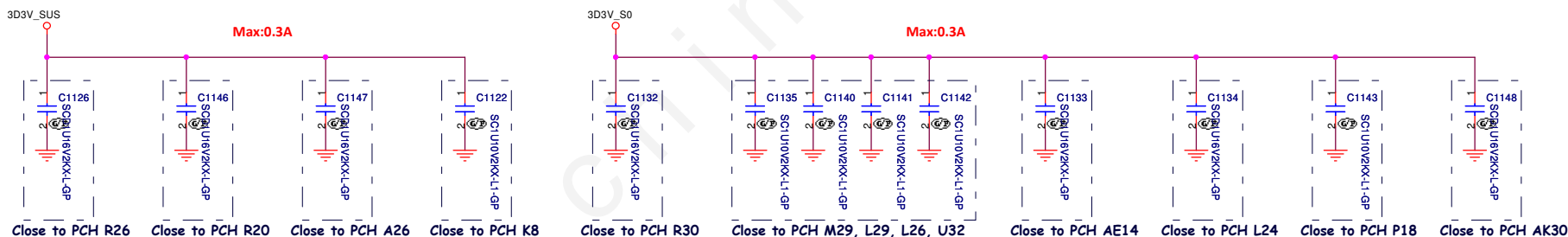
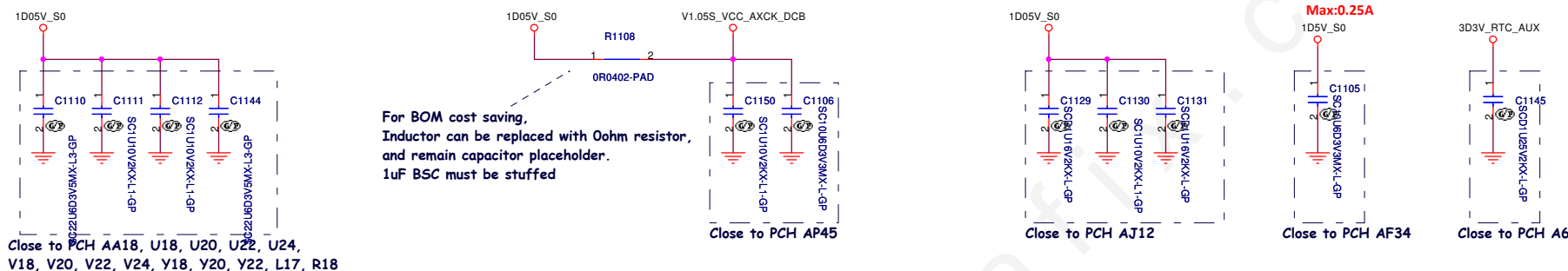
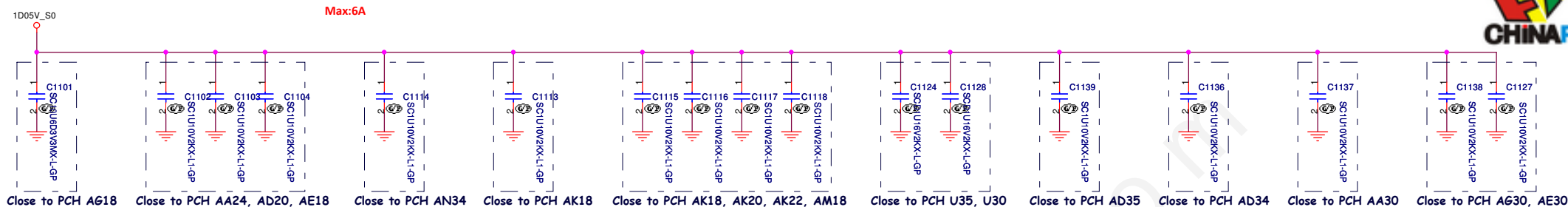


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Title CPU (Power CAP1)		
Size A4	Document Number Poseidon 860M	Rev -1
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Title		
CPU (Power CAP2)		
Size A3	Document Number	Rev
	Poseidon 860M	-1
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SSID = MEMORY

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS# DIMM0 1

Layout Note:
Place these Caps near
SO-DIMMA.

SODIMMA A DECOUPLING

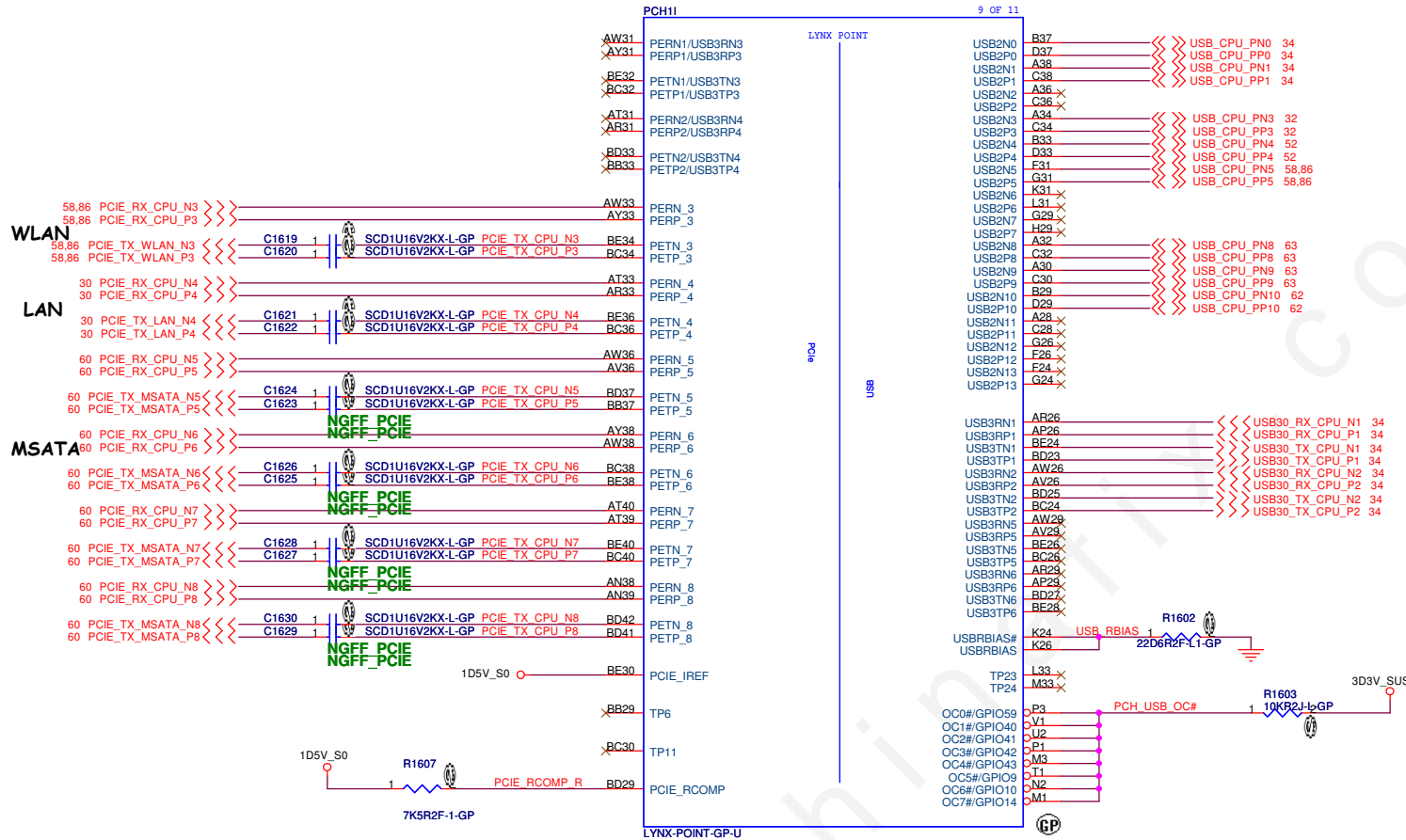
Place these caps
close to VTT1 and
VTT2.

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SSID = PCH

USB Table

Pair	Device
0	USB3.0(port0)
1	USB3.0(port1)
2	
3	Card Reader
4	CCD
5	Mini Card1 (WLAN)
6	TOUCH PANEL
7	
8	USB2.0
9	USB2.0
10	TOUCH PAD
11	
12	
13	



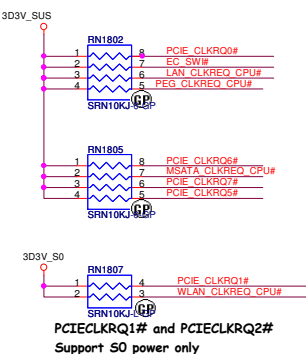
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Title CPU (PCI/USB)	
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SSID = PCH



WLAN

LAN

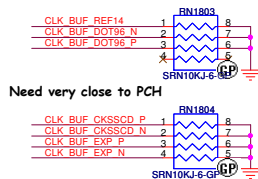
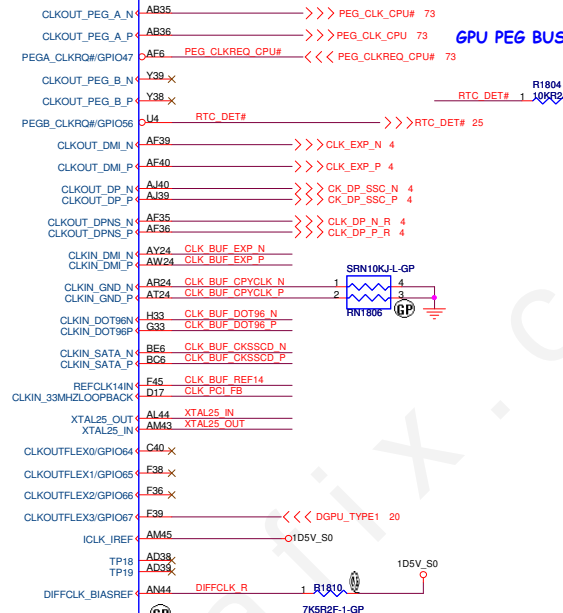
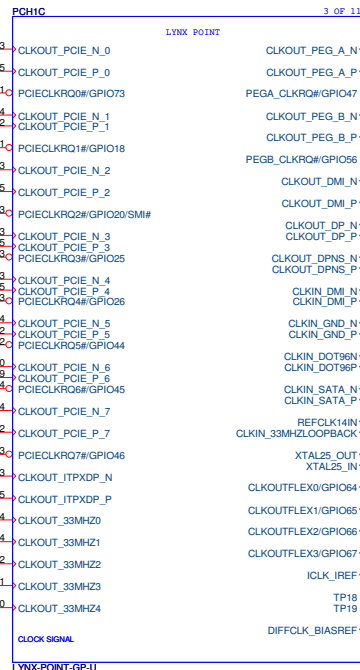
MSATA

88 CLK_PCI_TPM <<< 1 R1905 22R2J-L1-GP CLK_PCI_TPM R E44

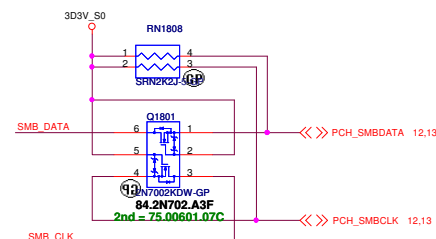
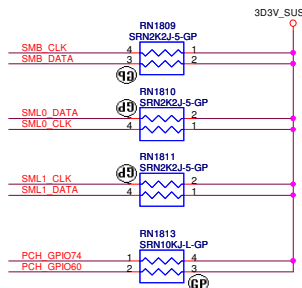
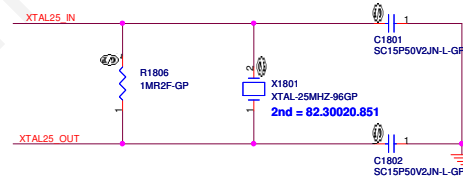
CLK_PCI_FB 1 R1905 22R2J-L1-GP CLK_PCI_FB R B42

65 CLK_PCI_LPC <<< 1 R1905 22R2J-L1-GP CLK_PCI_LPC R F41

24 CLK_PCI_KBC <<< 1 R1905 22R2J-L1-GP CLK_PCI_KBC R A40



Need very close to PCH

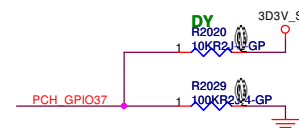
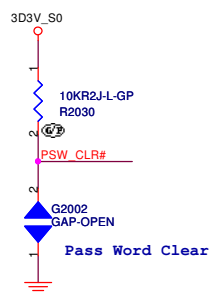
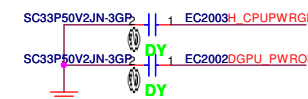
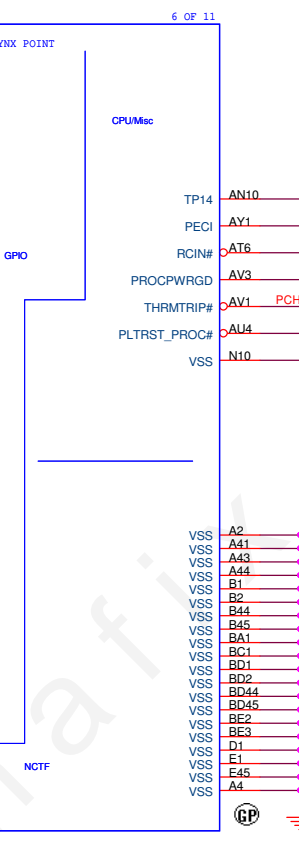
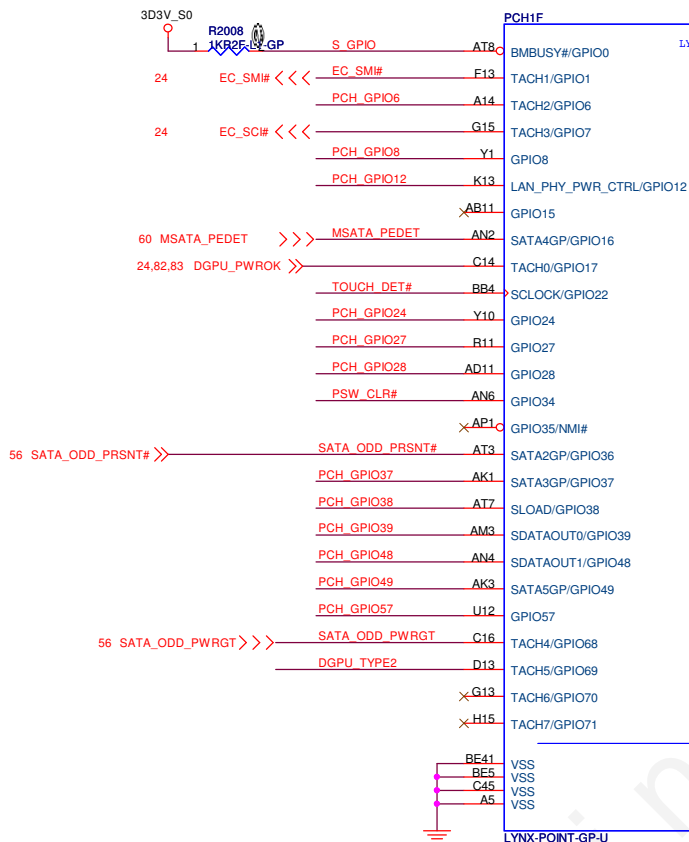
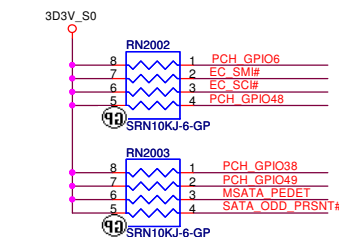
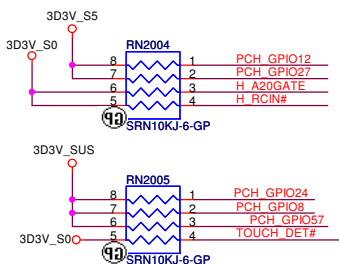


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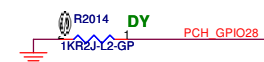
<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.</p>			
Title			
CPU (PCI-E/SMBUS/CLOCK/CL)			
Size	Document Number		Rev
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SSID = PCH



TLS Confidentiality

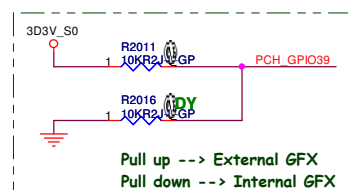
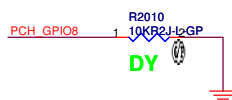
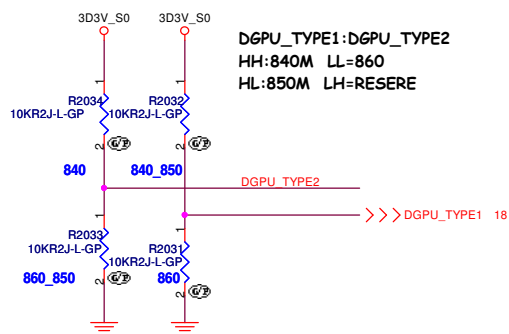
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)



PLL ON DIE VR ENABLE

ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2013 STUFFED)

DGPU_TYPE1:DGPU_TYPE2
HH:840M LL=860
HL:850M LH=RESERE

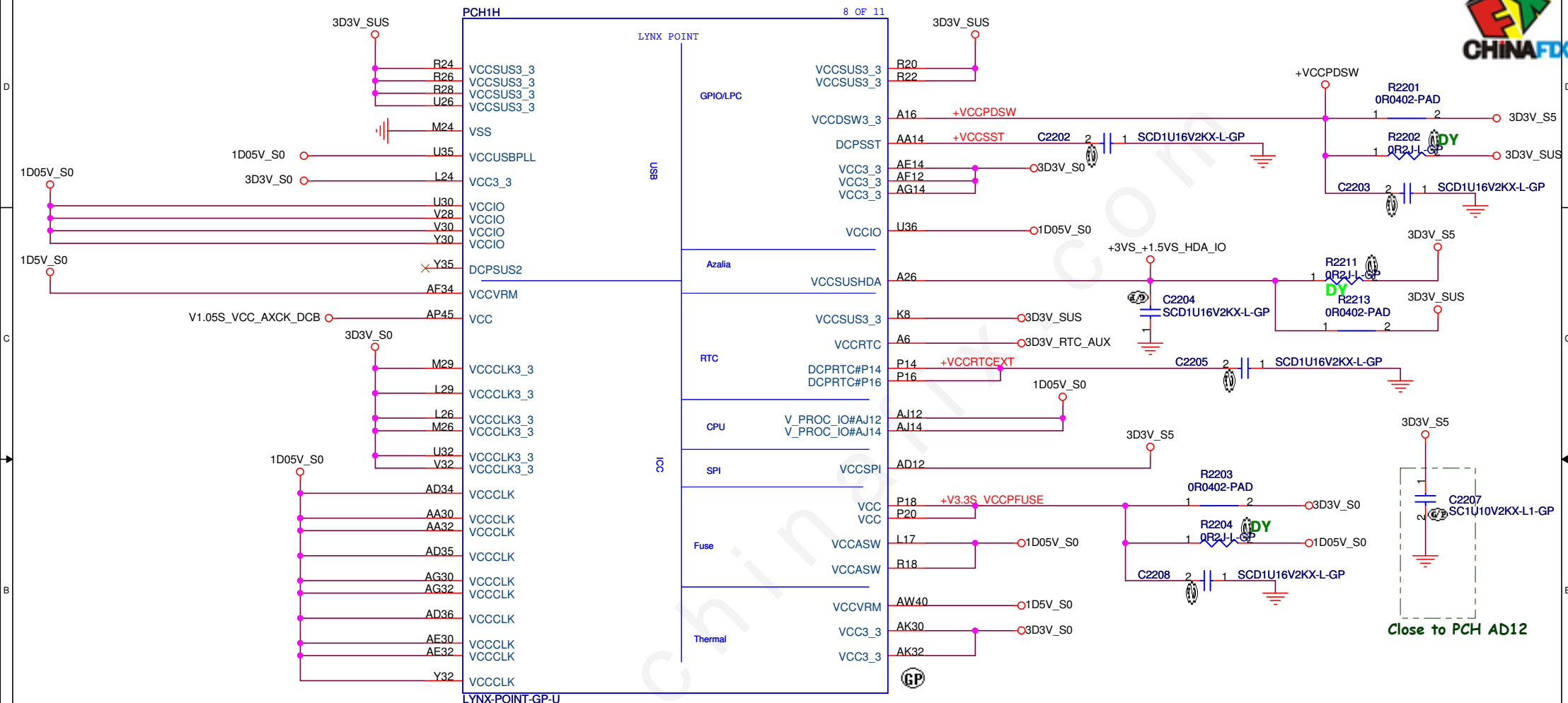


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Title		
CPU (GPIO/MISC)		
Size A3	Document Number	Rev -1
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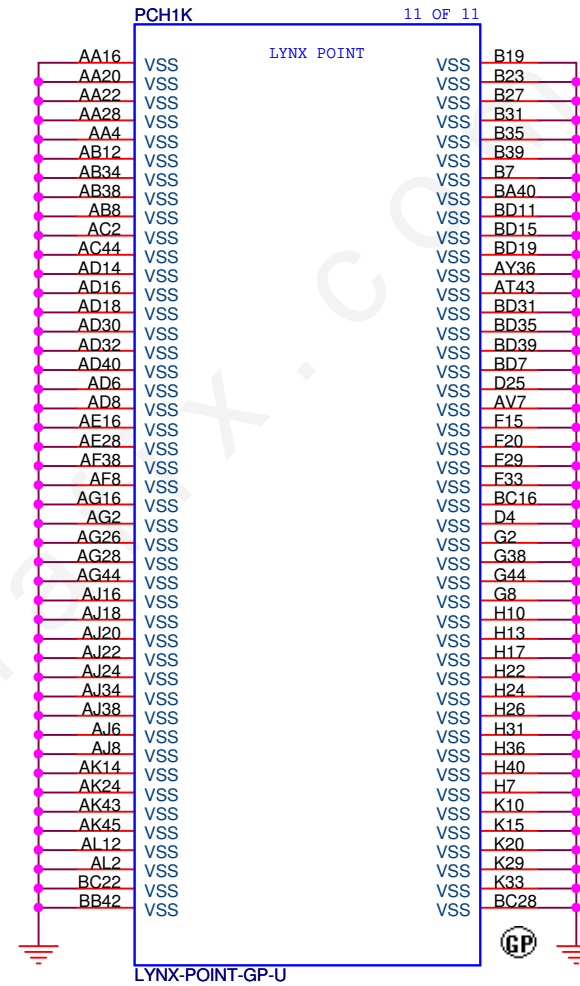
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Title			
CPU (RSVD)			
Size	Document Number		Rev
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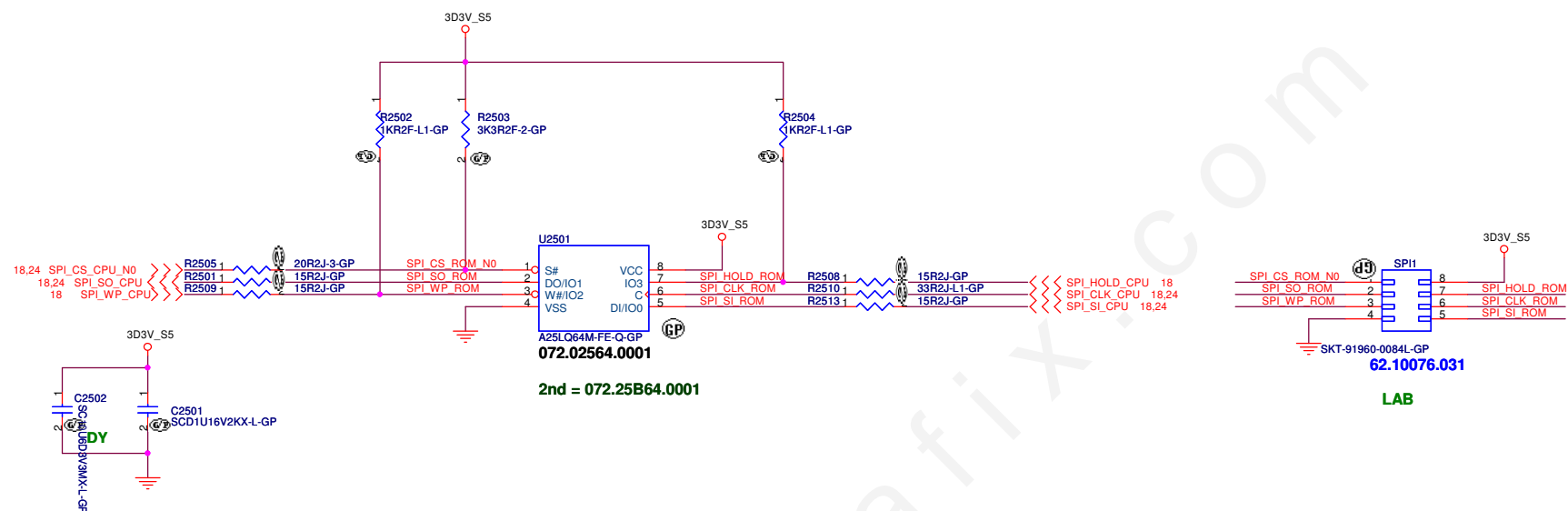
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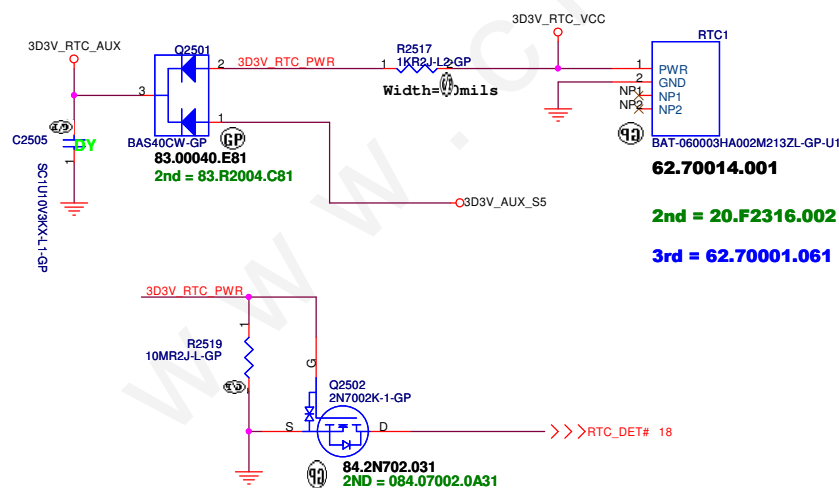
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil



SSID = RBAT



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Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
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SSID = Thermal

Thermal sensor NCT 7718W

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
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84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

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2nd = 84.T3904.H11
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2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2nd = 84.T3904.H11
84.T3904.C11

2.System Sensor, Put on palm rest

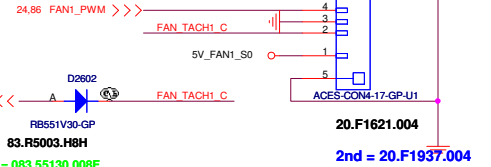
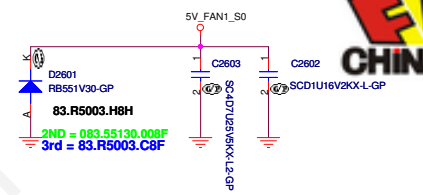
Layout Notice:

Layout notice:
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

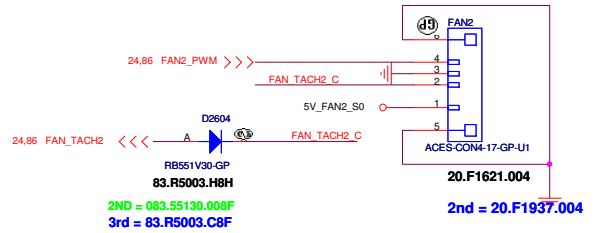
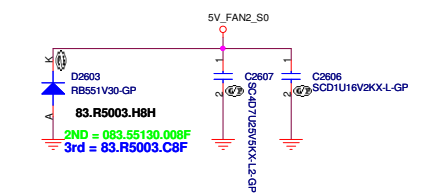
074.00788.00B9
1.H/W T8 Shutdown
T8=85 degree

ADB (Active Dusting Blower) function

Layout 15 mil



Layout 15 mil



ALERT# /T CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T8=85 degree T_CRIT temperature strapping point

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Title	Document Number	Rev
Thermal 7718/Fan Controller P2793	Poseidon 860M	-1
Date: 1/26/2014	Sheet 26 of 102	

<http://vinofix.vn>

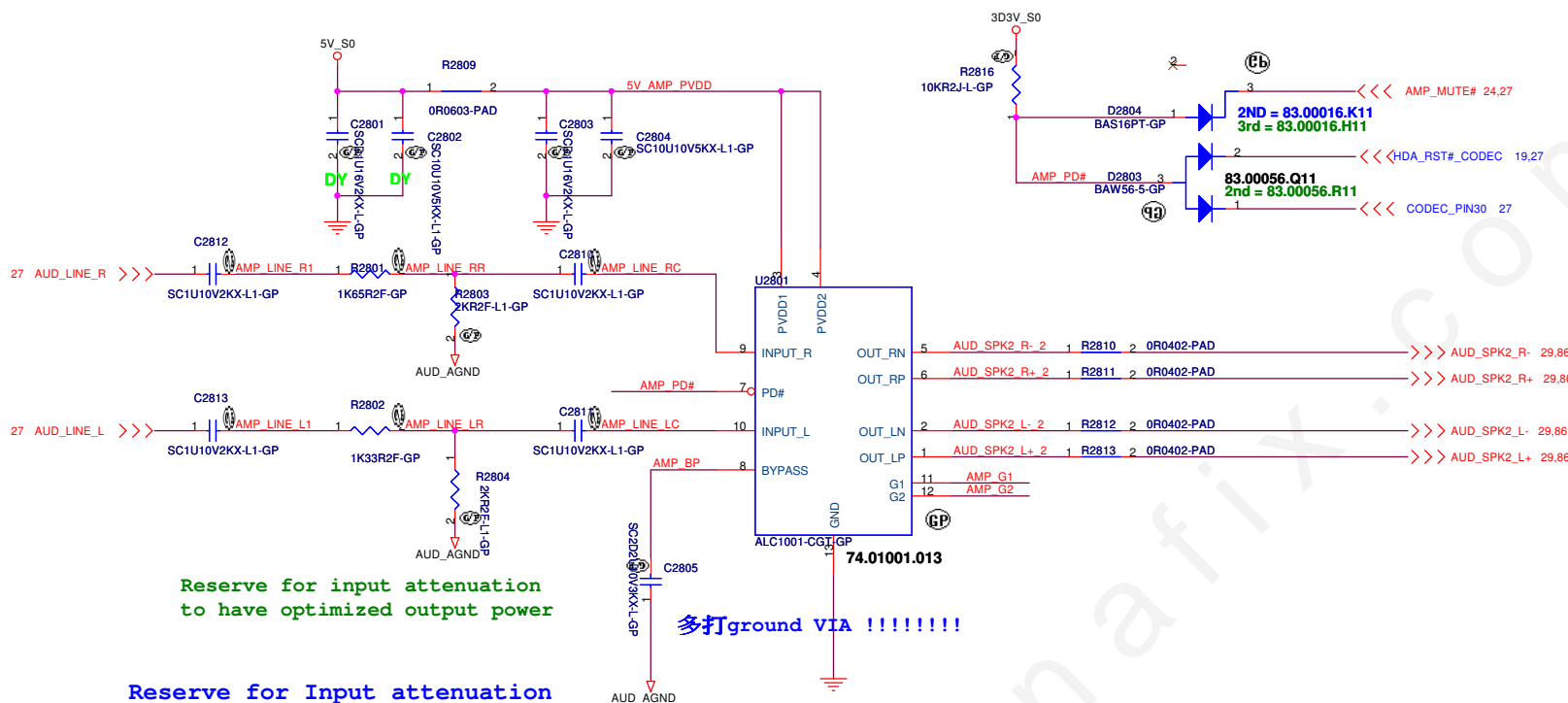
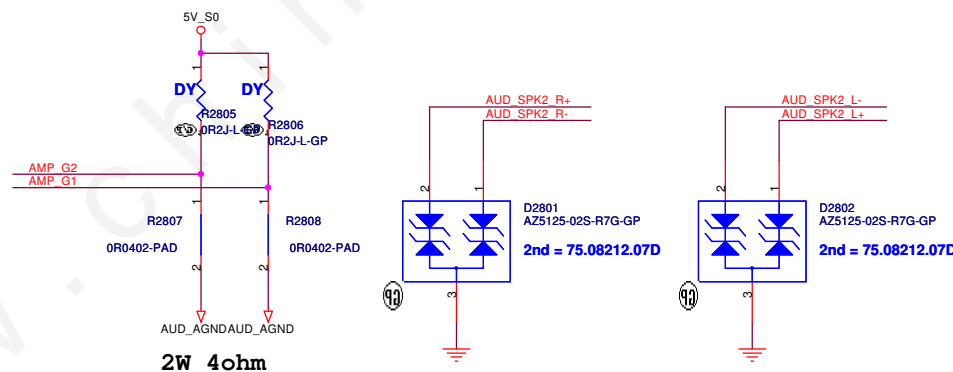


Table 6. Amplifier Gain

G2	G1	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

*Condition is at 5V/40hm

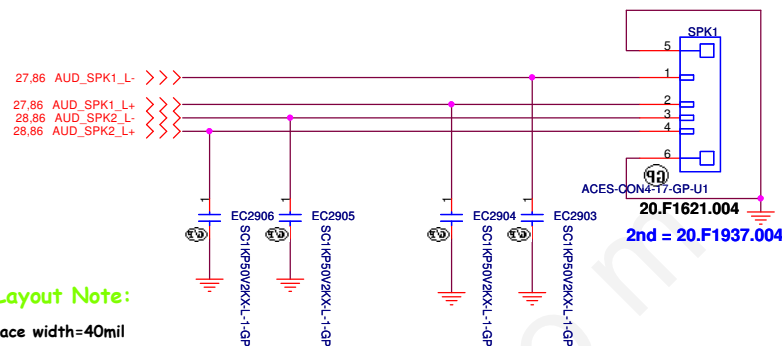
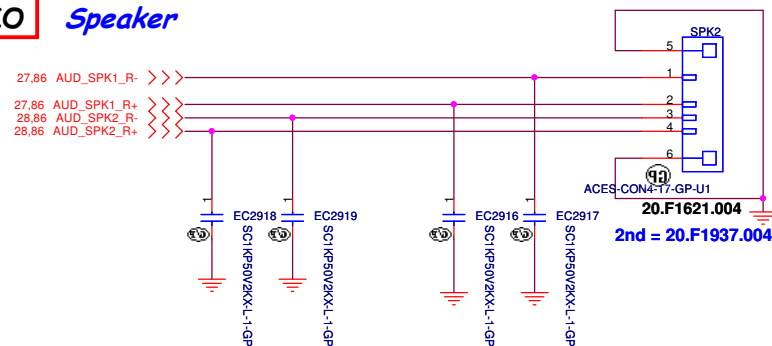


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SSID = AUDIO

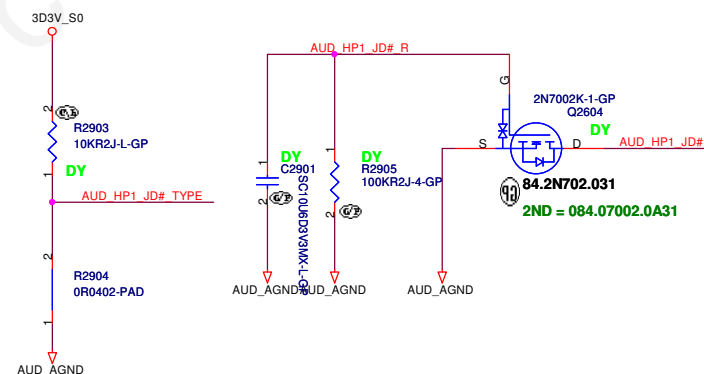
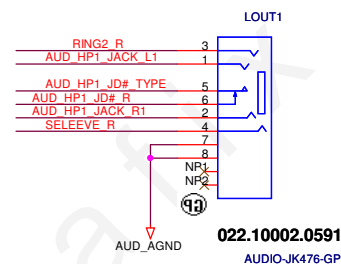
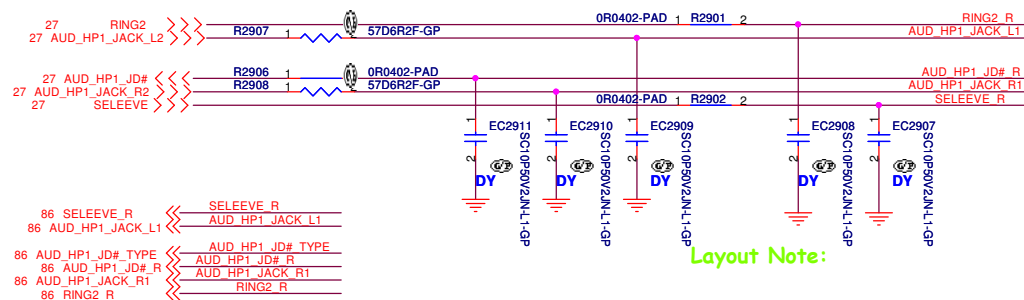
Speaker



Layout Note:
Trace width=40mil

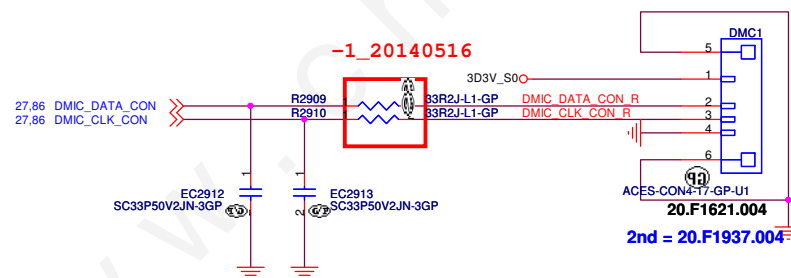


Combo Jack



Layout Note:

DMIC



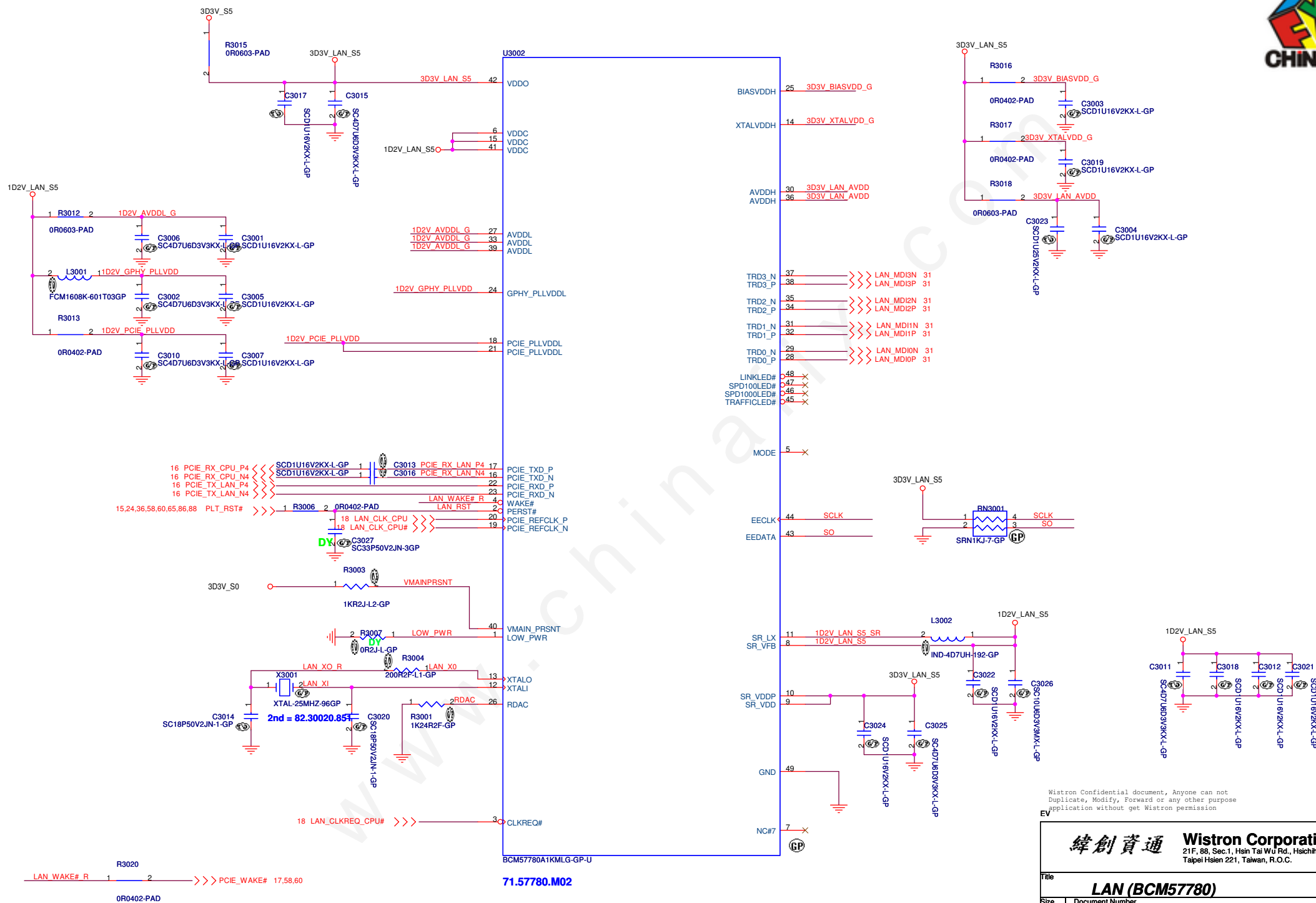
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Title	Audio Jack	Rev	-1
Size	Document Number		
Custom	Poseidon 860M		
Date:	Tuesday, June 17, 2014	Sheet	29 of 102

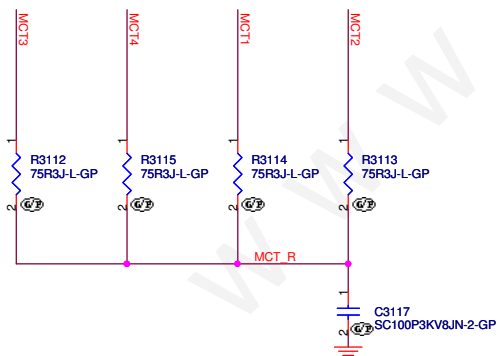
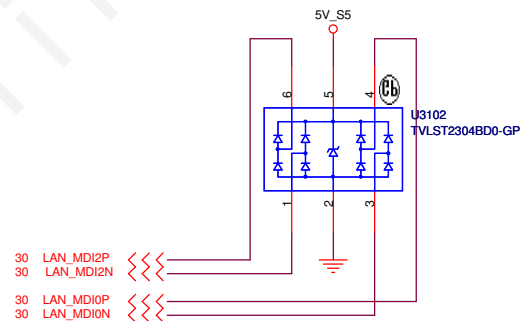
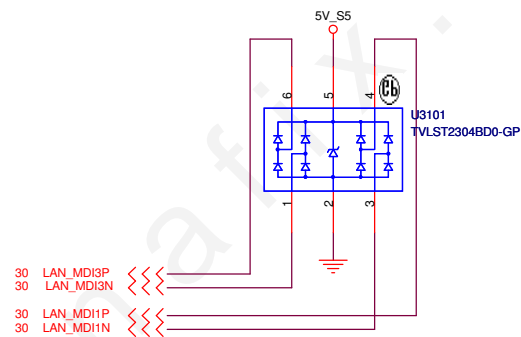
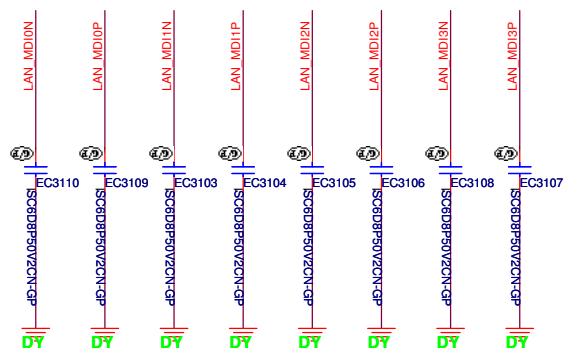
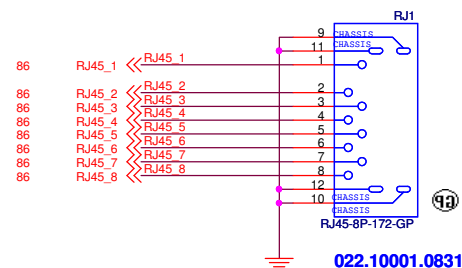
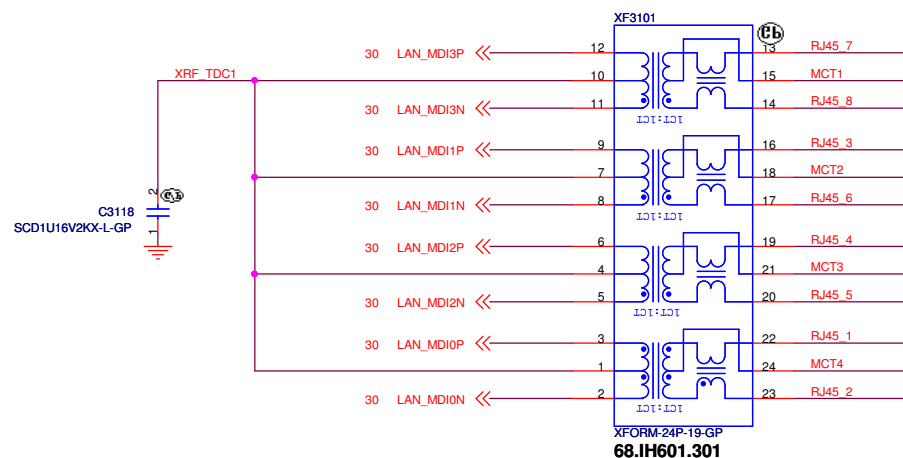
<http://vinofix.vn>



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Title LAN (BCM57780)	
Size A3	Document Number Poseidon 860M
Date Tuesday, June 17, 2014	Rev -1
Sheet 30	of 102

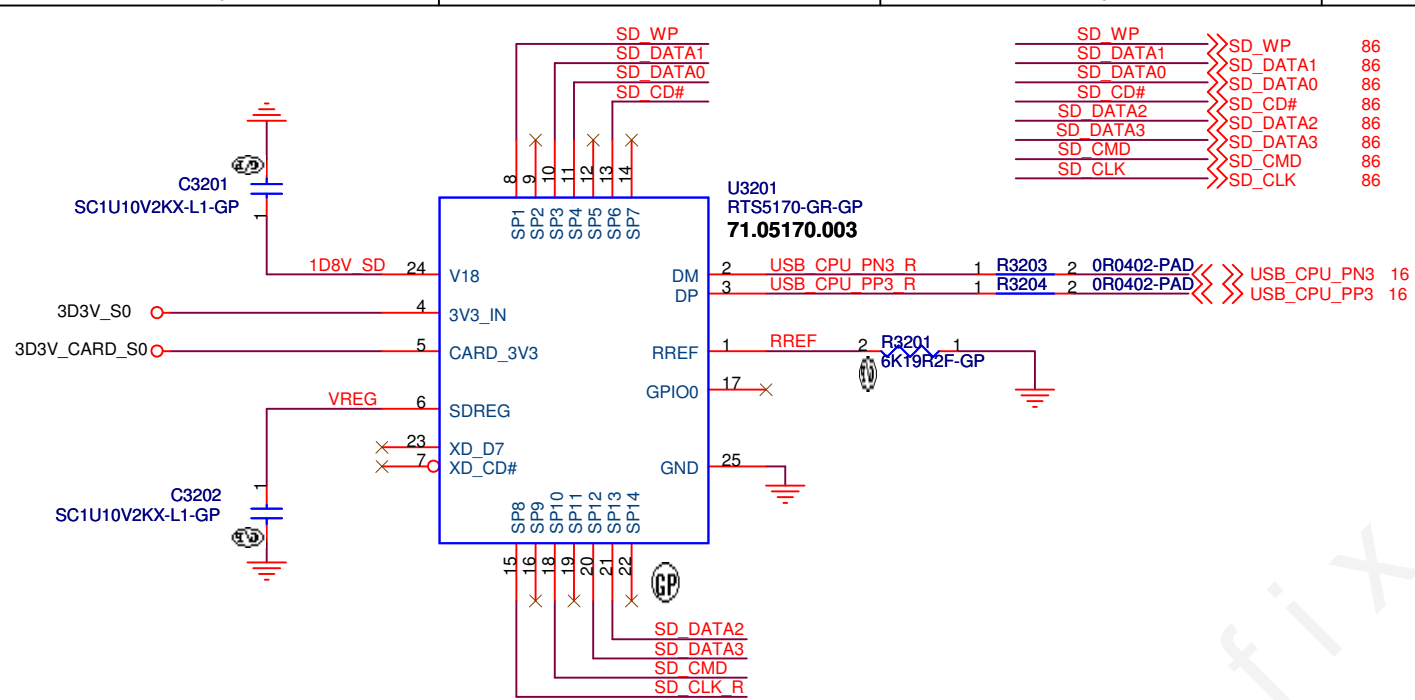
SSID = LAN



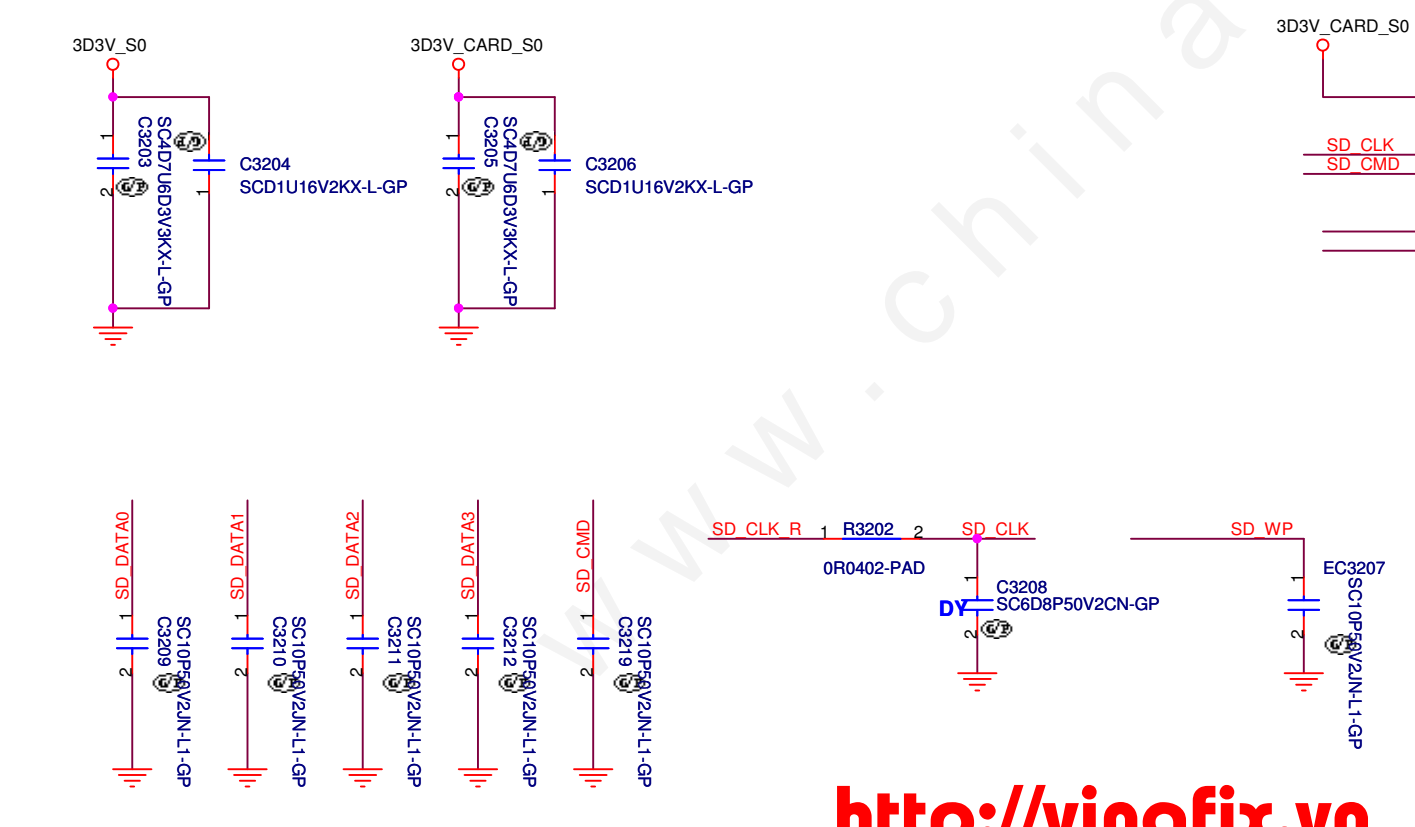
<http://vinofix.vn>

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Title: (LAN+VGA) CONNECTOR	
Size: Custom Date: Tuesday, June 17, 2014	Document Number: Poseidon 860M Sheet: 31 of 102
Rev: -1	



SP1	XD_CD#	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



2nd = 62.10051.C41

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Title

RTS5170 (CARD READER)

Size A4

Document Number

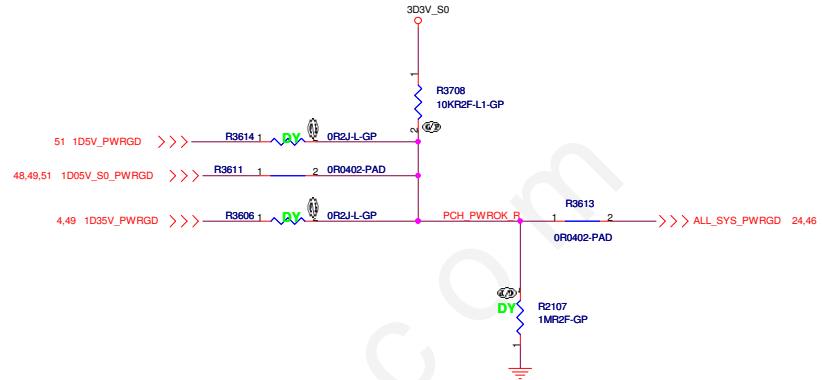
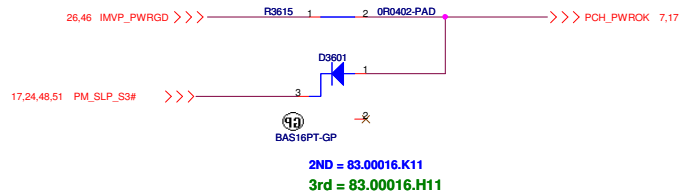
Poseidon 860M

Rev -1

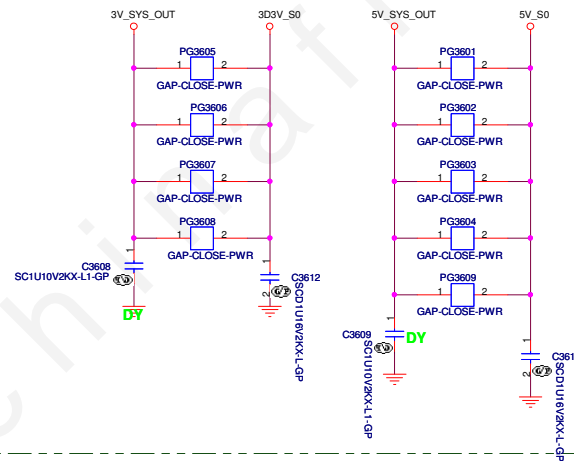
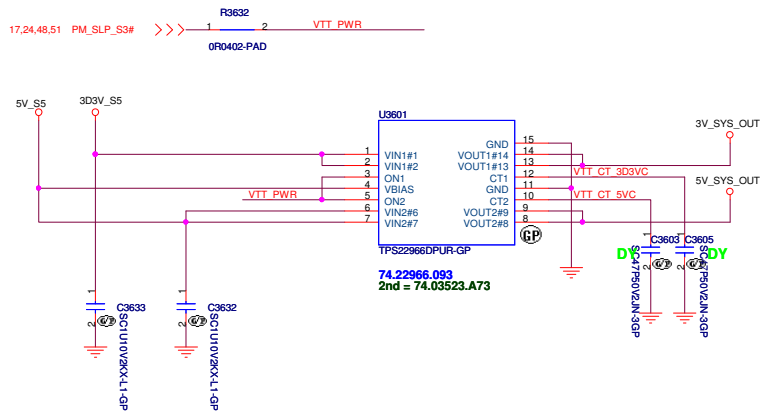
Date: Tuesday, June 17, 2014

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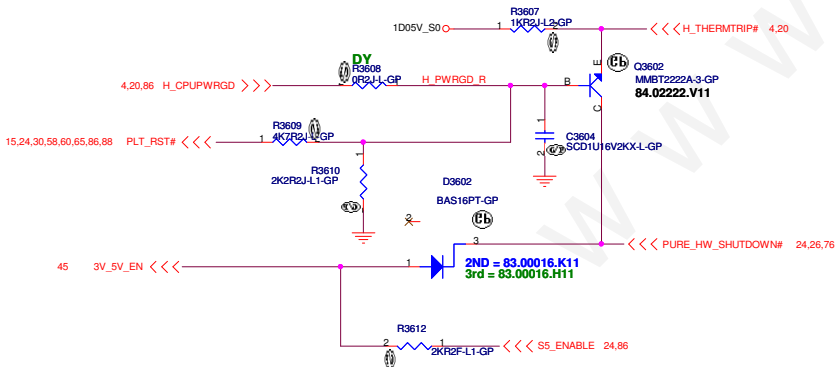
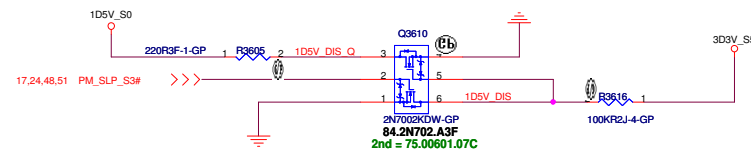
Power Sequence



ANNIE Run Power



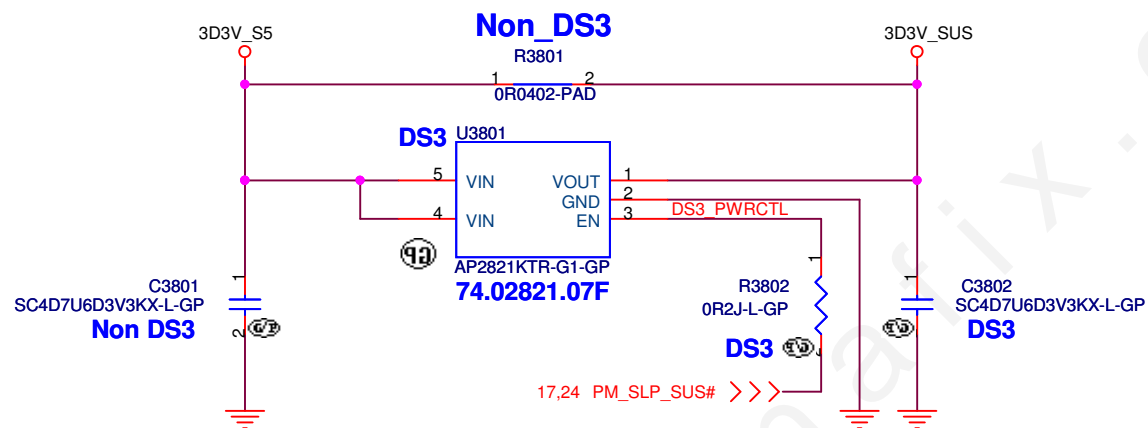
Discharge circuit



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File	Power Plane Enable & SEQUENCE
Size	Document Number
Custom	Poseidon 860M
Date	1/26/2014, June 17, 2014
Sheet	36 of 102
Rev	-1



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Title

DS3

Size
A4

Document Number

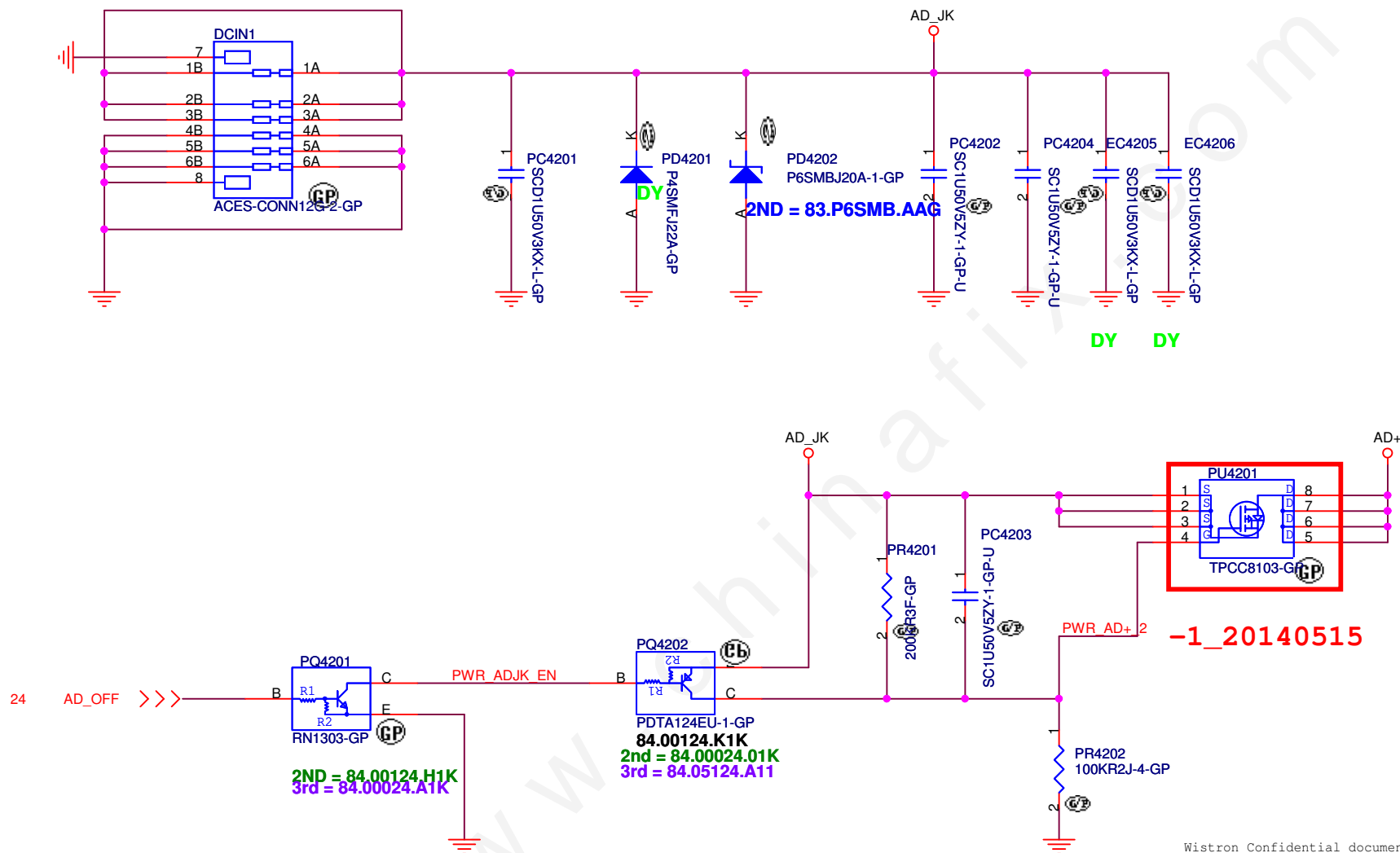
Poseidon 860M

Rev
-1

Date: Tuesday, June 17, 2014

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Adaptor in to generate DCBATOUT



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Title

DCIN JACK

Size
A4

Document Number

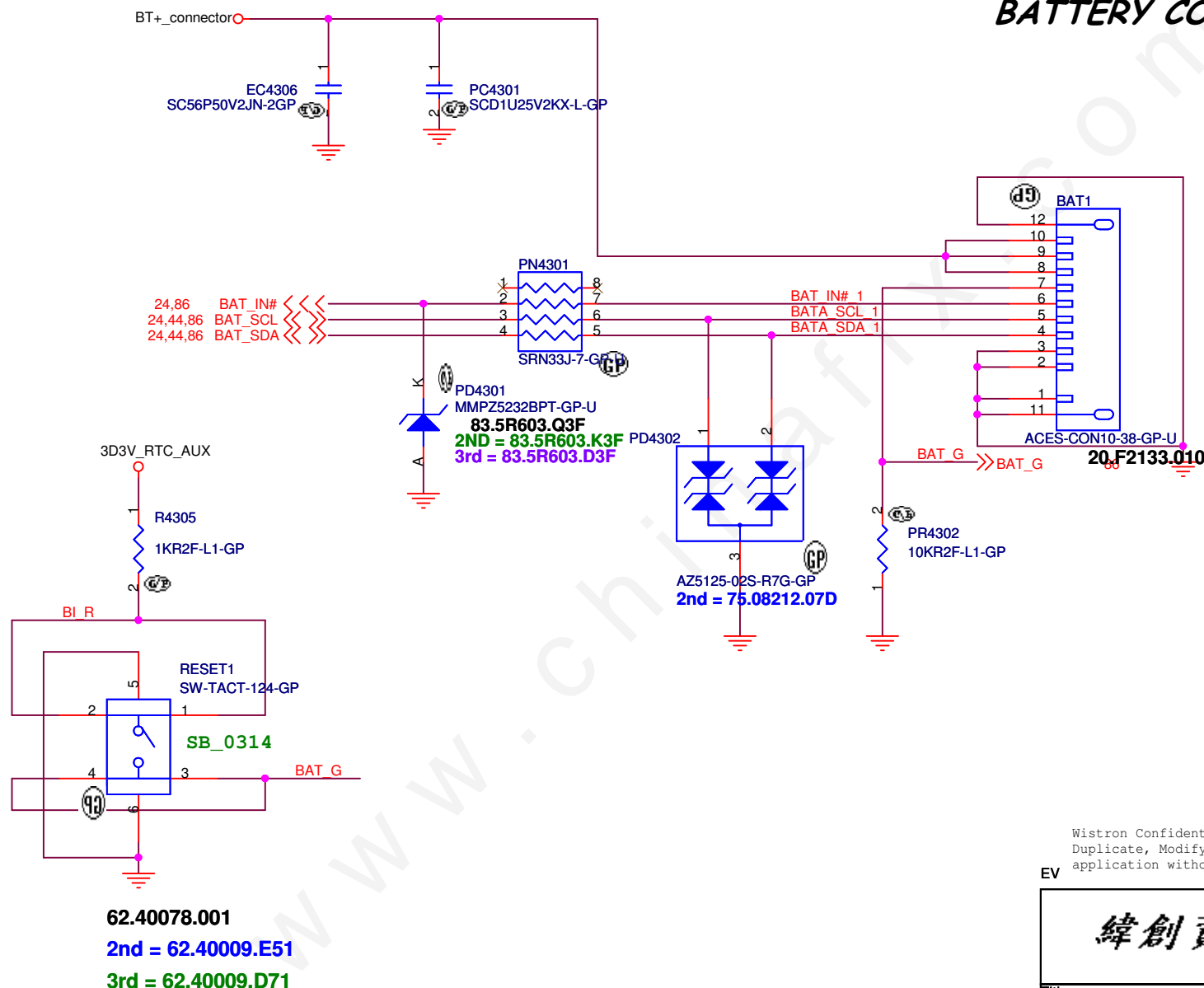
Poseidon_860M

Rev
-1

Date: Tuesday, June 17, 2014

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BATTERY CONNECTOR

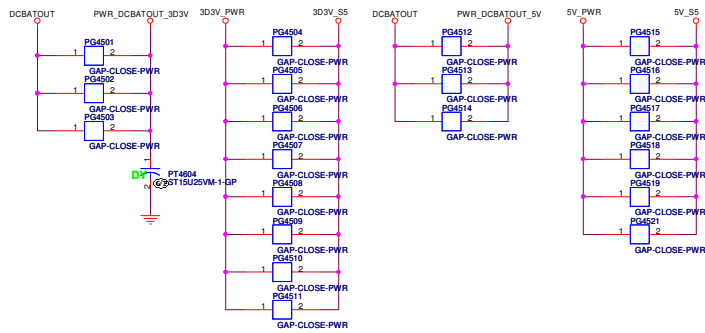


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Title		
BATT CONN		
Size A4	Document Number Poseidon 860M	Rev -1
Date: Tuesday, June 17, 2014	Sheet 43	of 102



High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

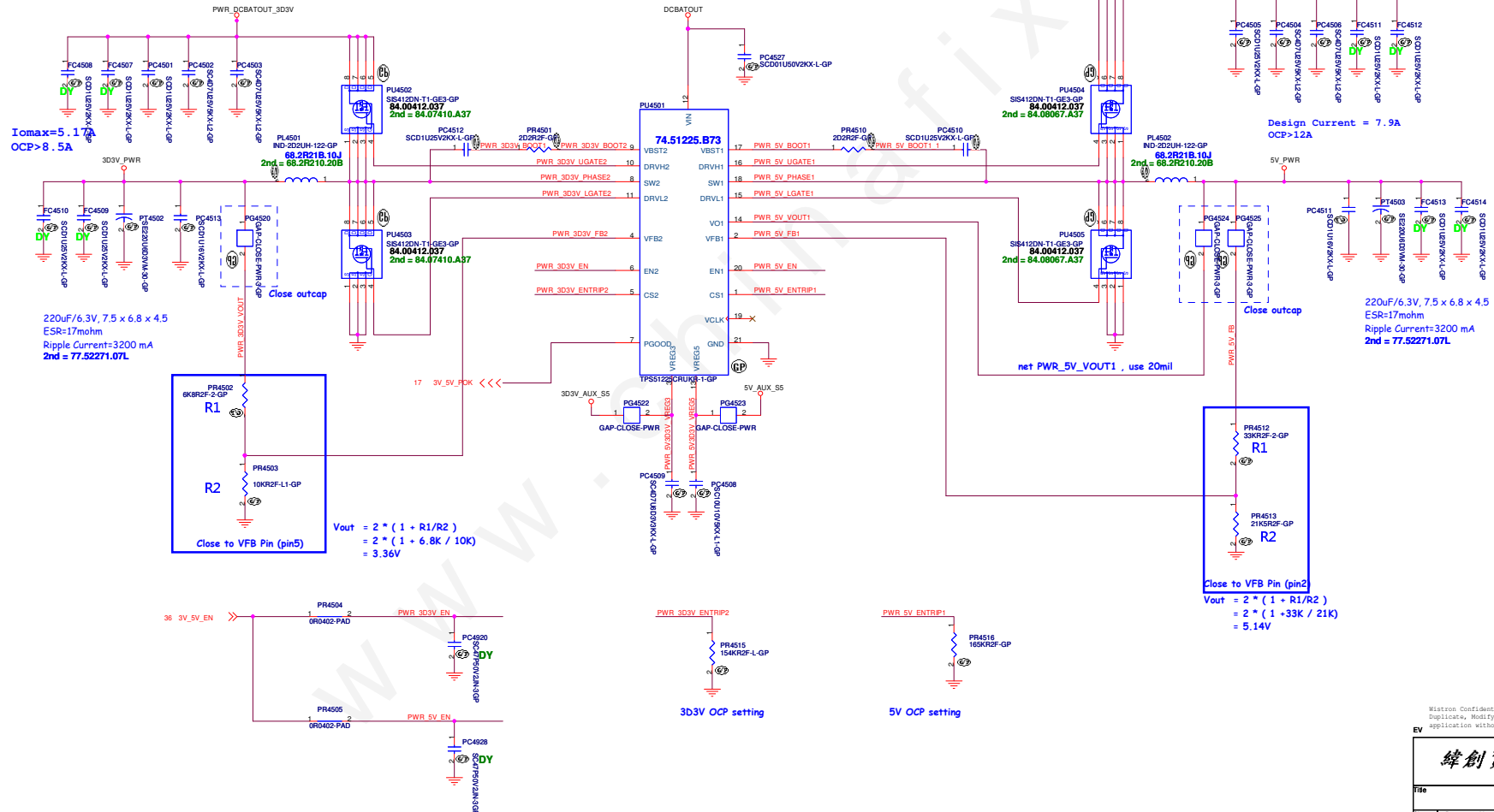
Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

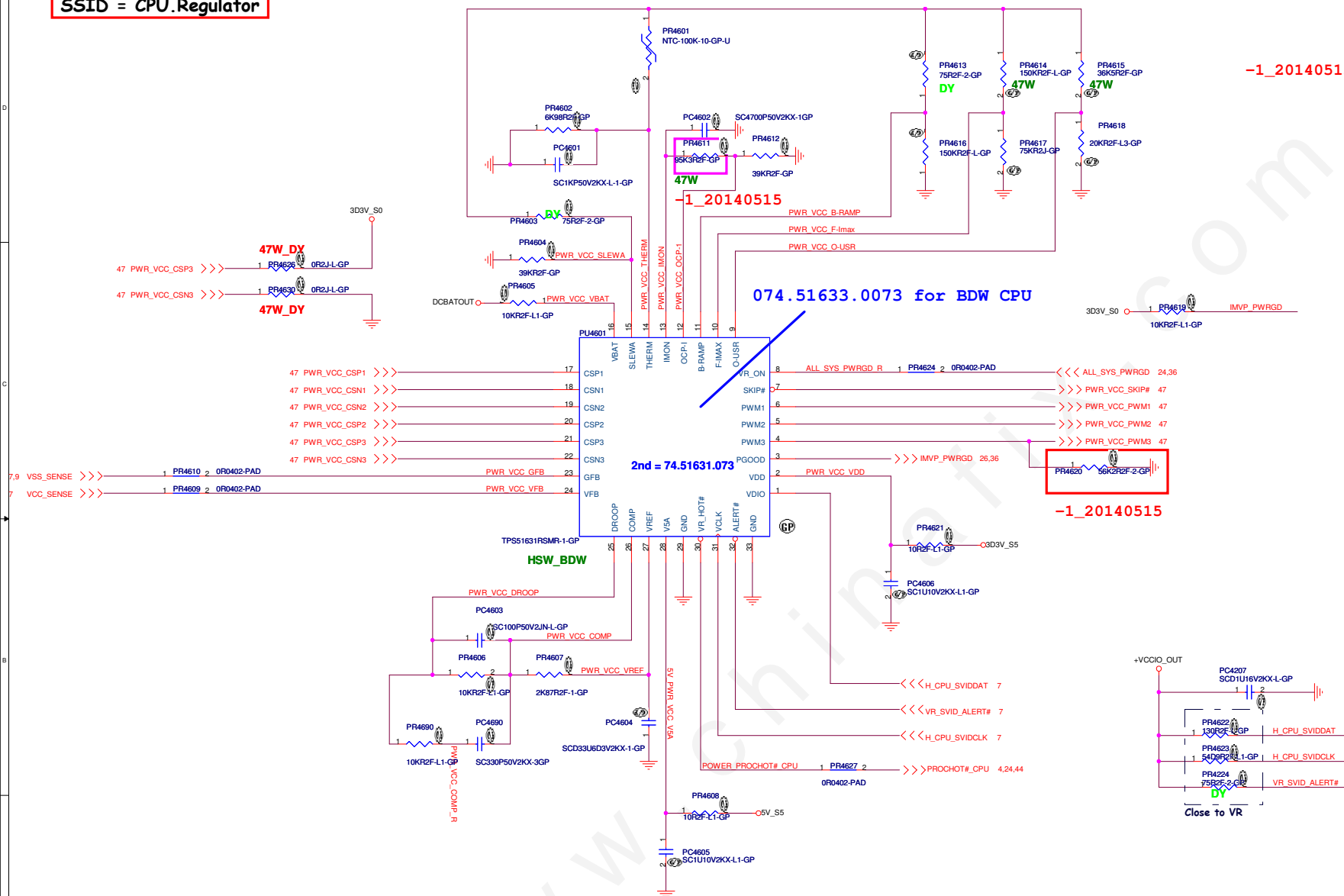
Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A



SSID = CPU.Regulator

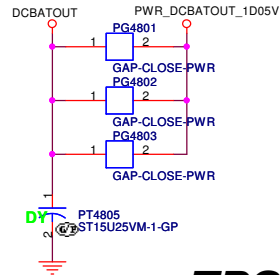


	47W
PC4602	4.7nF
	78.47224.2FL
PR4611	95.3k
	64.95325.6DL
PR4614	150k
	64.15035.6DL
PR4617	75k
	63.75334.1DL
PR4615	36.5k
	64.36525.6DL
PR4618	20k
	64.20025.6DL
PR4626	DY
PR4630	DY
PR4602	6.98k
	64.69815.6DL
PR4607	2.87k
	64.28715.6DL



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Title			
TPS51361 CPUCORE(1/2)			
Size	Document Number	Rev	
Custom	Poseidon 840M	-1	
Date:	100609, June 17, 2014	Sheet	46 of 102

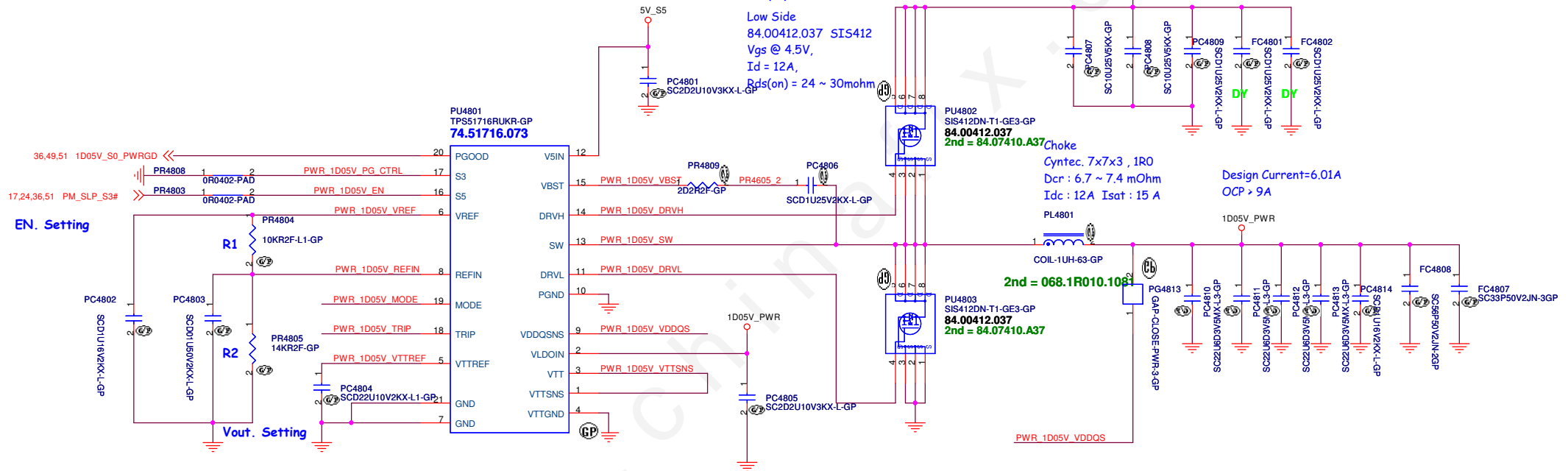
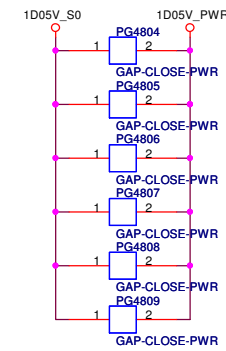
<http://vinafix.vn>



TPS51716 for 1D05V

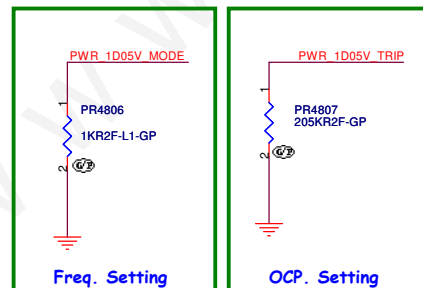
High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



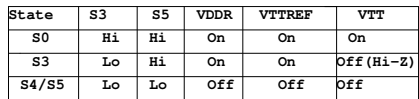
MODE	PR5006	Frequency	Discharge Mode
	33k ohm	500kHz	Non-tracking Discharge
	22k ohm	670kHz	
	12k ohm	670kHz	
	1k ohm	500kHz	Tracking Discharge

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

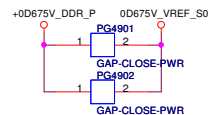


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Title: DC to DC 1D05V(TPS51716)	
Size: A3	Document Number: Poseidon 860M
Date: Wednesday, June 18, 2014	Sheet: 48 of 102



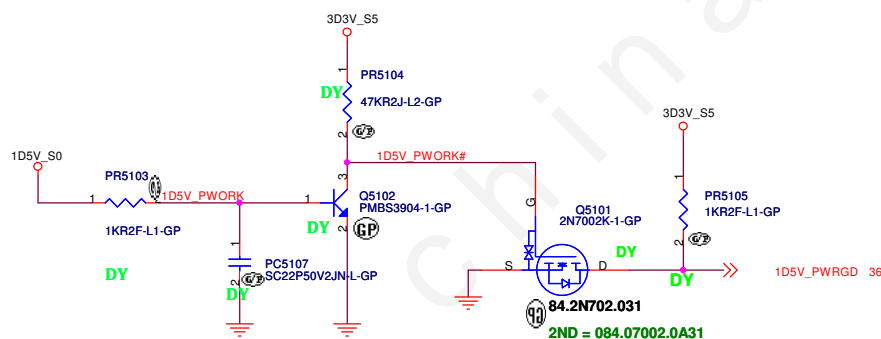
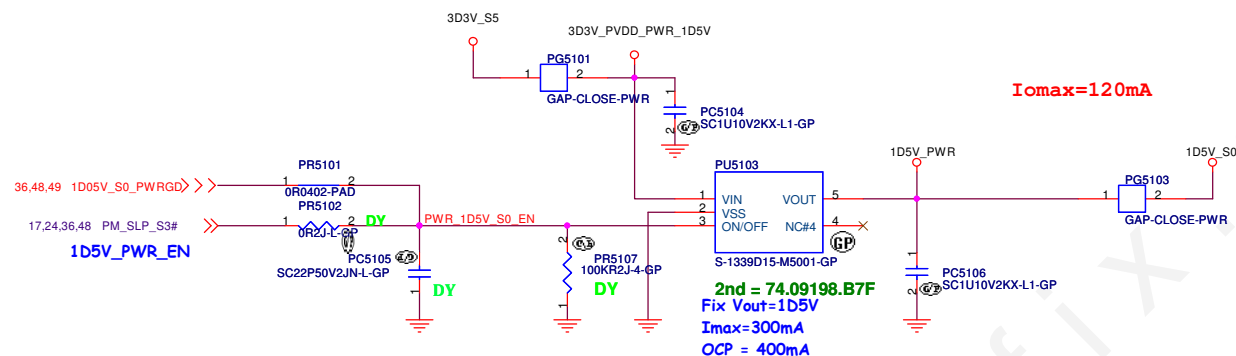
PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	
1k ohm	500kHz	Tracking Discharge



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Title			
TPS51716 (VDDQ VTT)			
Size Custom	Document Number		Rev -1
Poseidon 860M			
Date:	Wednesday, June 18, 2014	Sheet 49 of	102

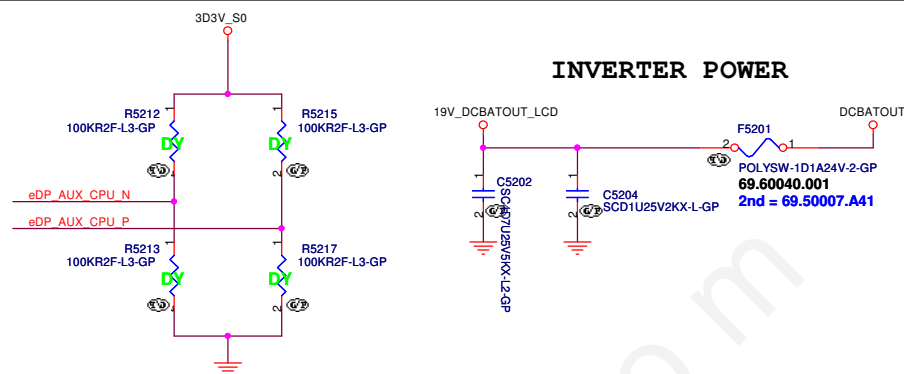
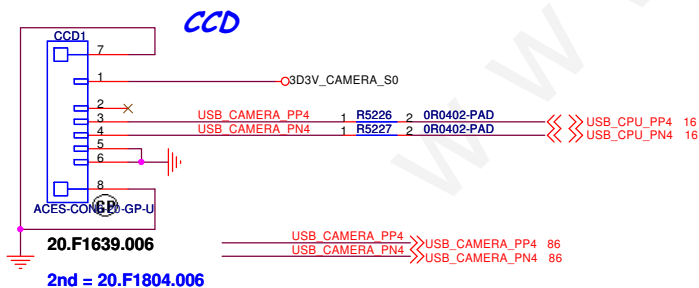
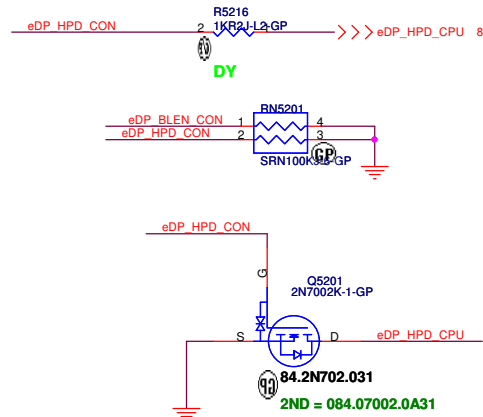
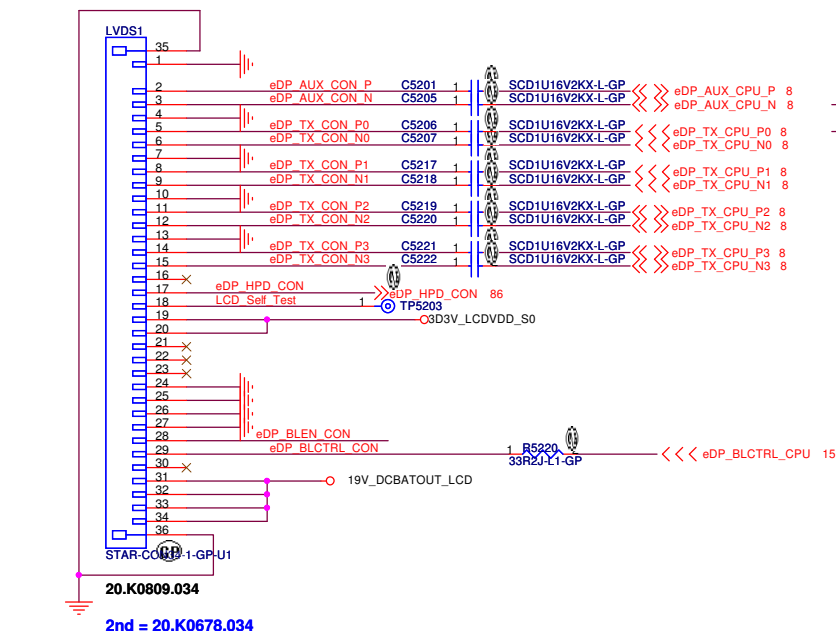
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



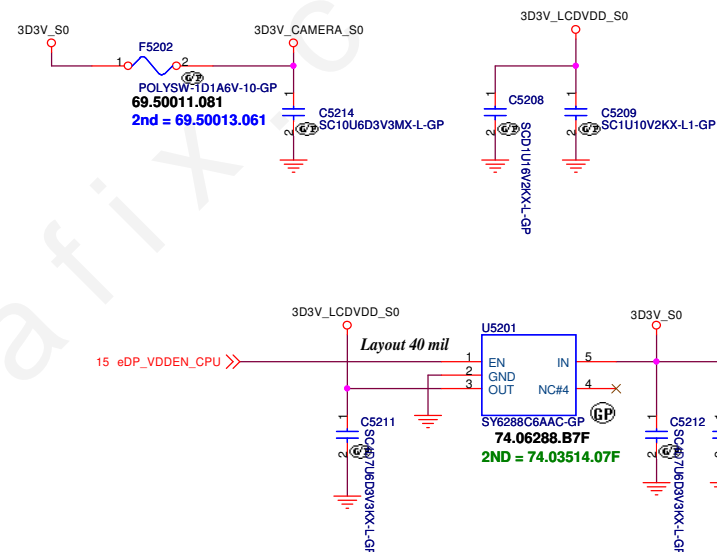
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Title		
1D5V_S0 TLV70215		
Size	Document Number	Rev
A3	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 51 of 102

SSID = VIDEO



Camera Power



eDP_AUX_CON_P >>> eDP_AUX_CON_P 86
eDP_AUX_CON_N >>> eDP_AUX_CON_N 86
eDP_TX_CON_P0 >>> eDP_TX_CON_P0 86
eDP_TX_CON_N0 >>> eDP_TX_CON_N0 86
eDP_TX_CON_P1 >>> eDP_TX_CON_P1 86
eDP_TX_CON_N1 >>> eDP_TX_CON_N1 86
eDP_TX_CON_P2 >>> eDP_TX_CON_P2 86
eDP_TX_CON_N2 >>> eDP_TX_CON_N2 86
eDP_TX_CON_P3 >>> eDP_TX_CON_P3 86
eDP_TX_CON_N3 >>> eDP_TX_CON_N3 86
eDP_HPDCON >>> eDP_HPDCON 86
eDP_BLENCON >>> eDP_BLENCON 86
eDP_BLCCTRL_CON >>> eDP_BLCCTRL_CON 86

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LCD Connector

Document Number

Rev
-1

Poseidon 860M

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of
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Tuesday, June 17, 2014

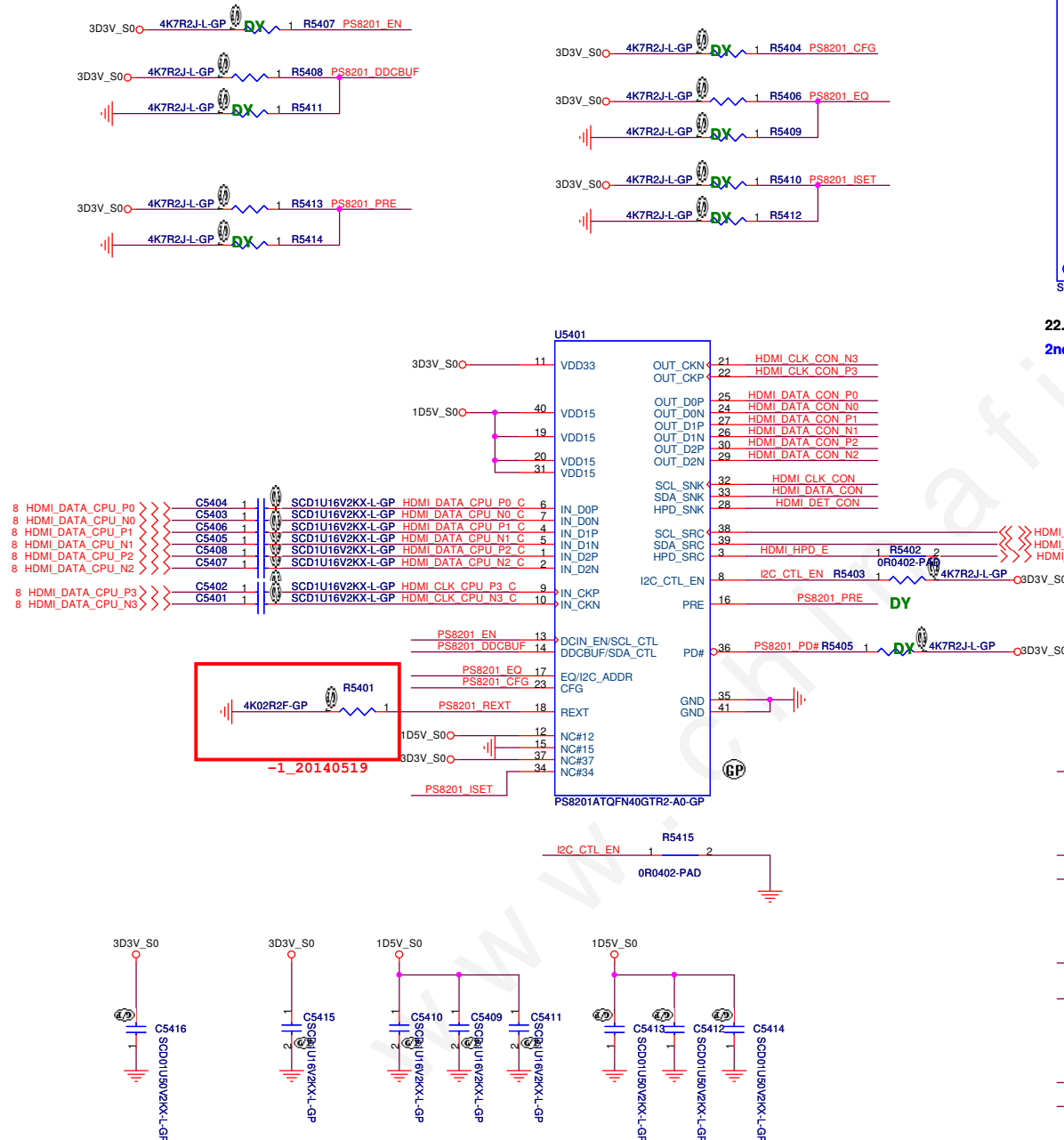
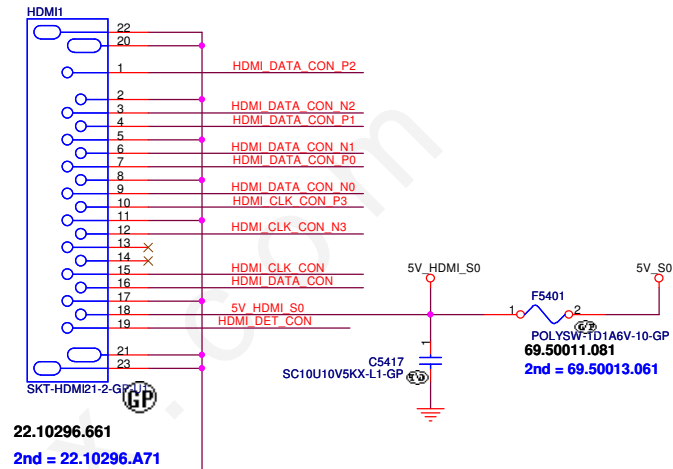
<http://vinafix.vn>

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN



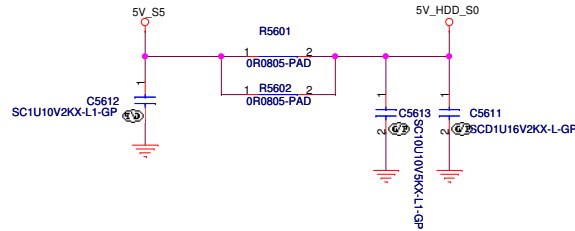
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EV		
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Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
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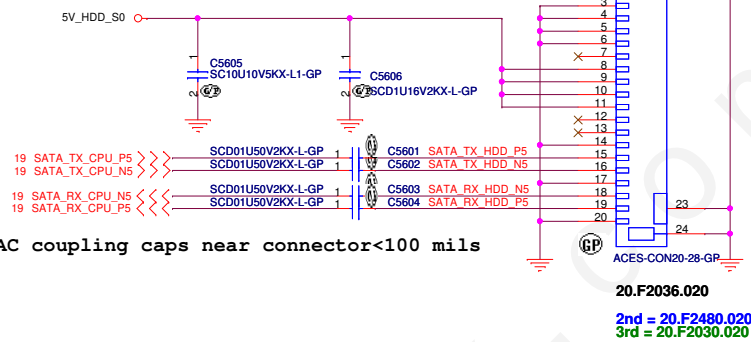
<http://vinofix.vn>

SSID = SATA

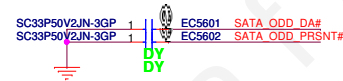
SATA HDD Connector



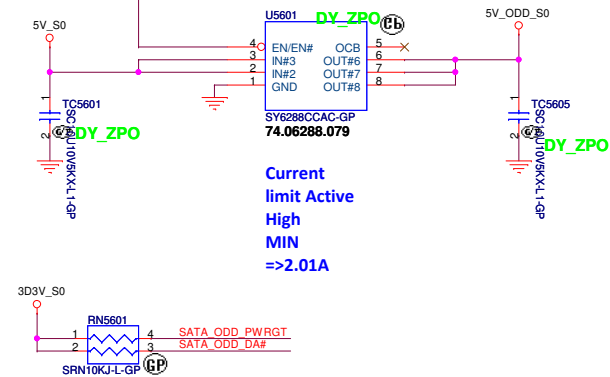
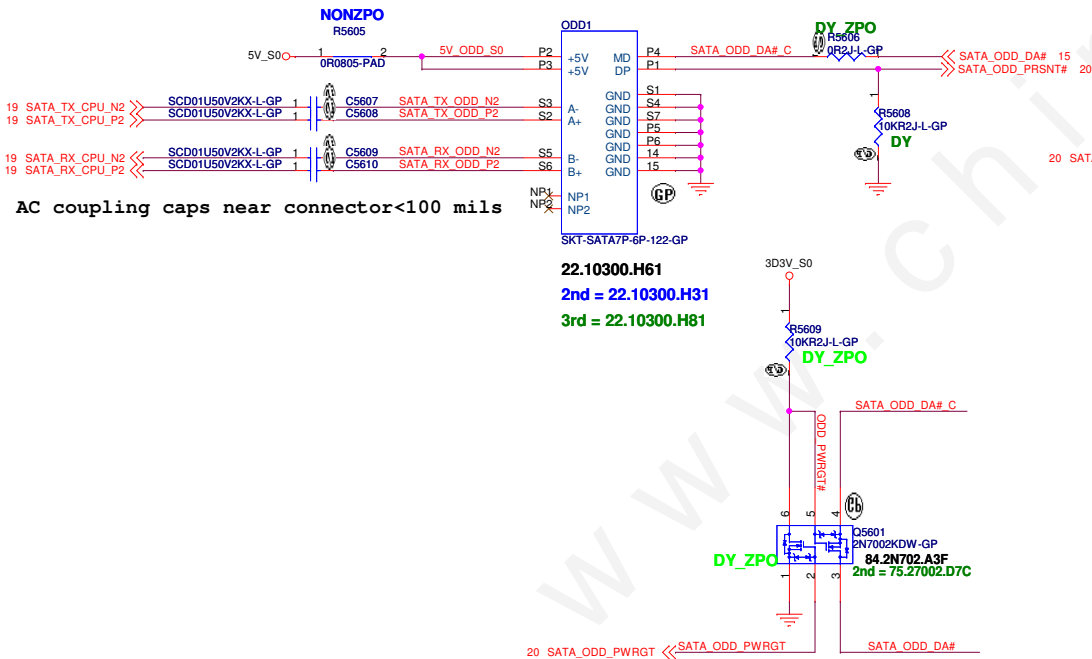
AC coupling caps near connector < 100 mils



ODD Connector



SATA Zero Power ODD

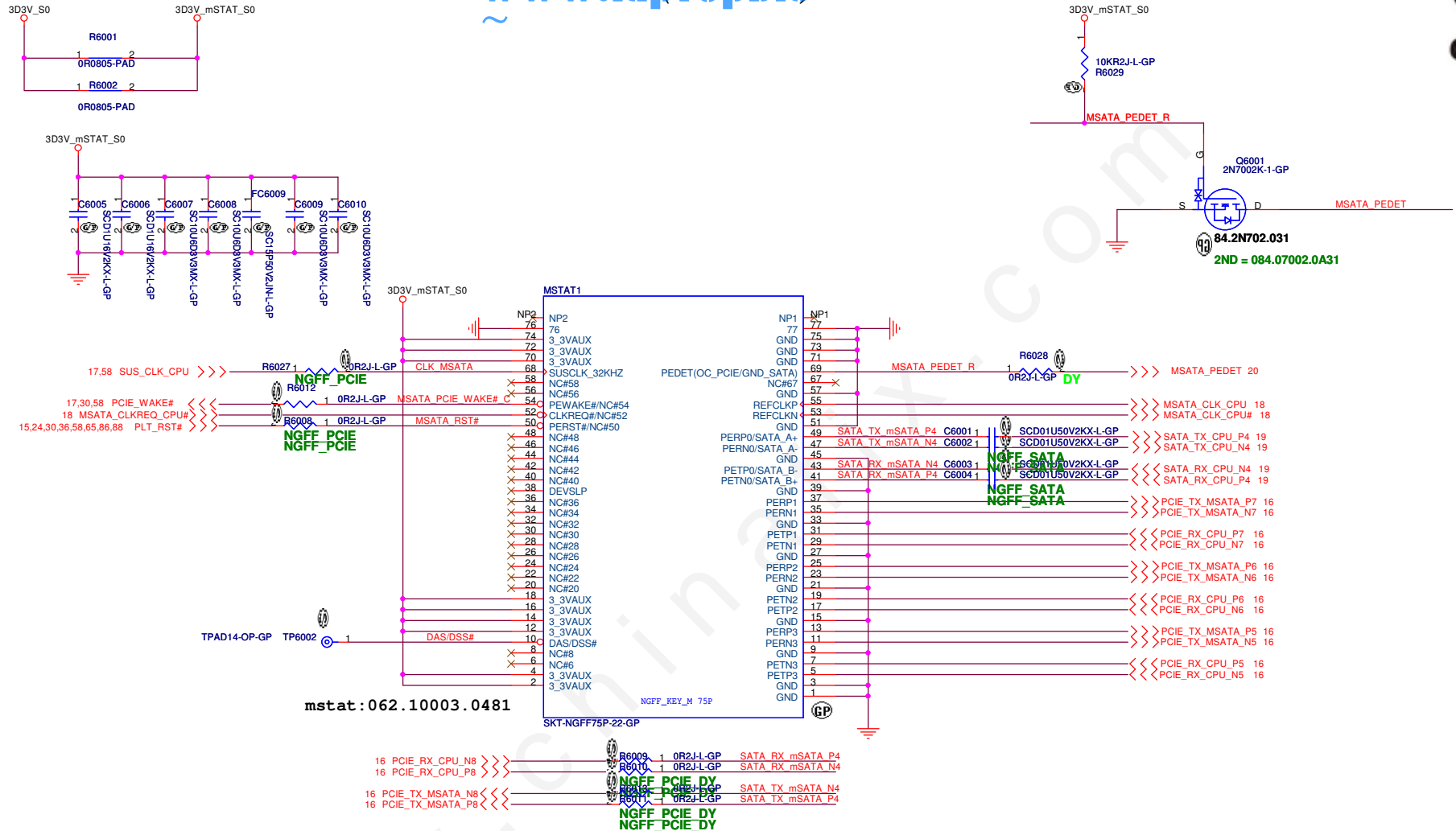


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EV		Title	
Size		Document Number	
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SSID = mSATA

Mini Card Connector(mSATA)



SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ³

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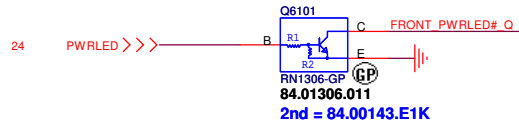
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Title: mSATA Connector	
Size: A3	Document Number: Poseidon 860M
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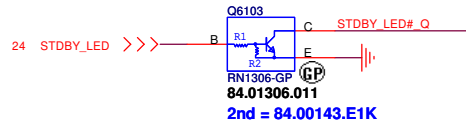
<http://vinofix.vn>

SSID = User.Interface

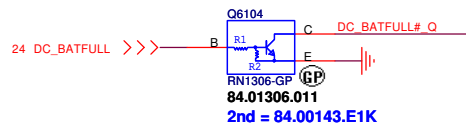
Power button LED



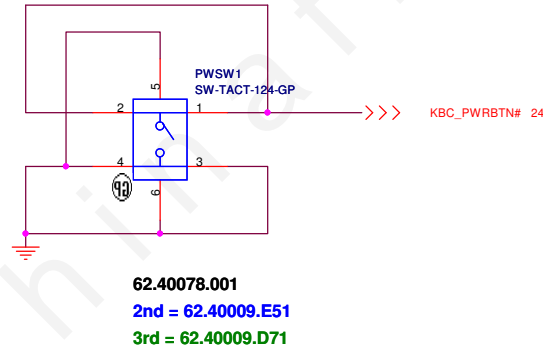
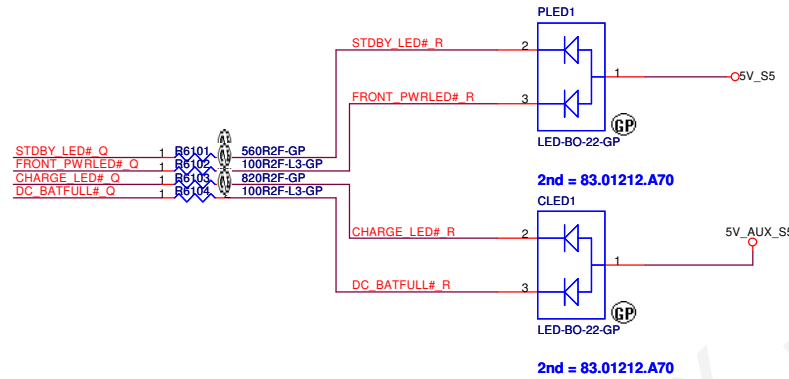
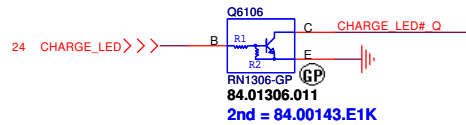
Power STDBY_LED



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

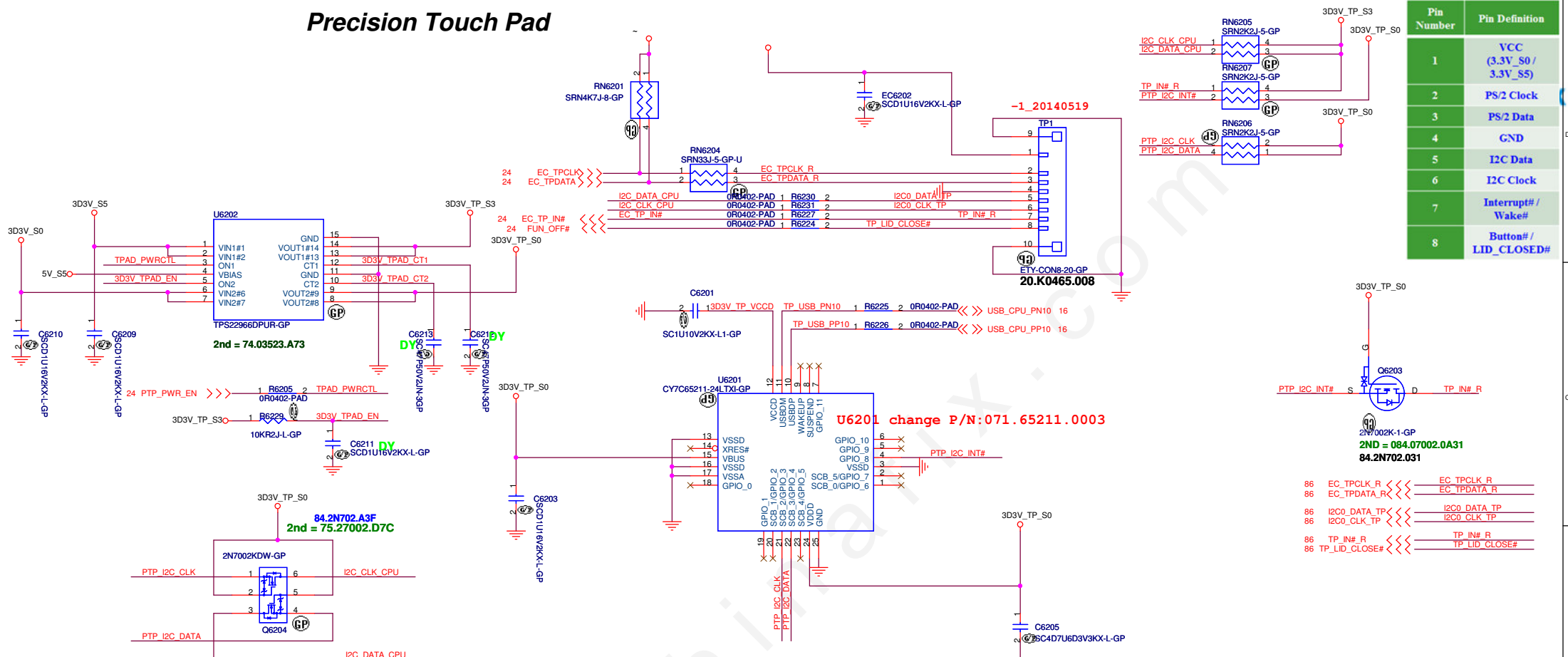


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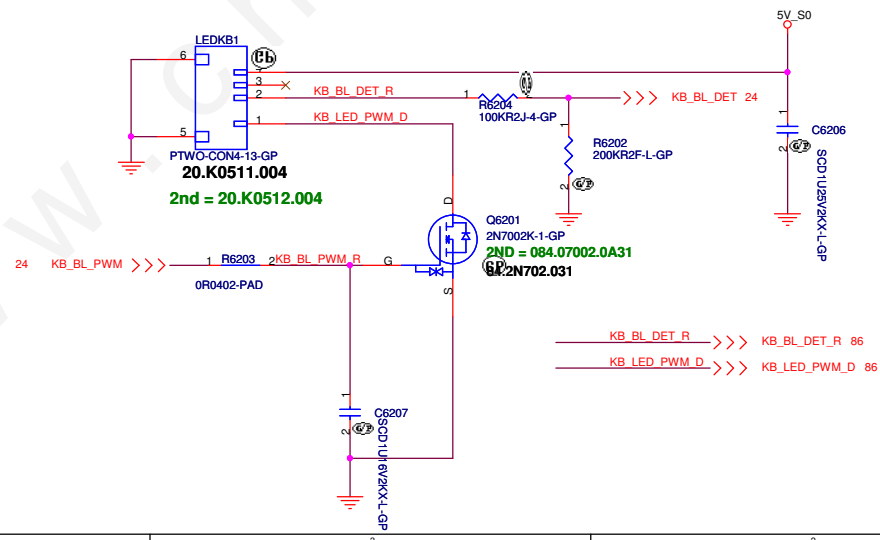
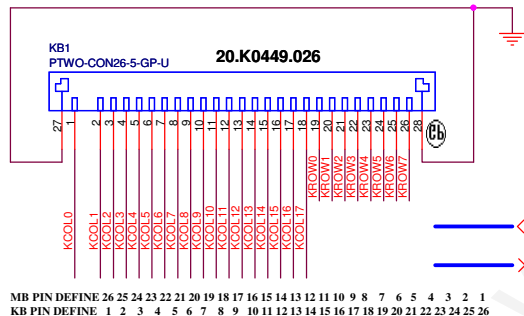
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		21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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LED Bard/Power Button			
Size A3	Document Number		Rev -1
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Precision Touch Pad

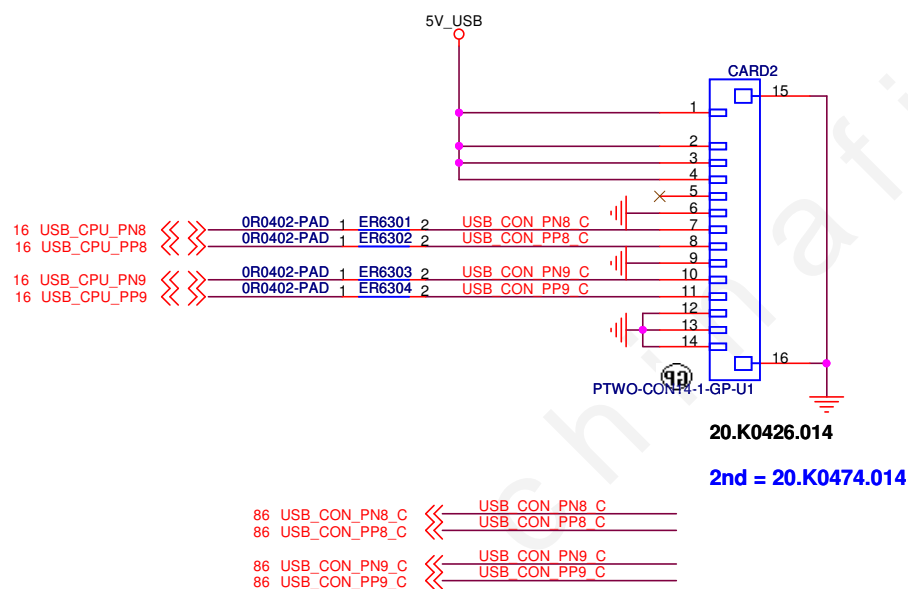
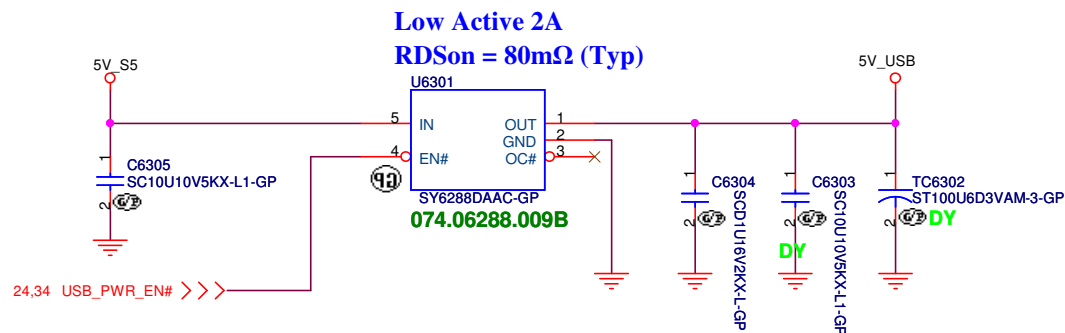


Internal Keyboard Connector



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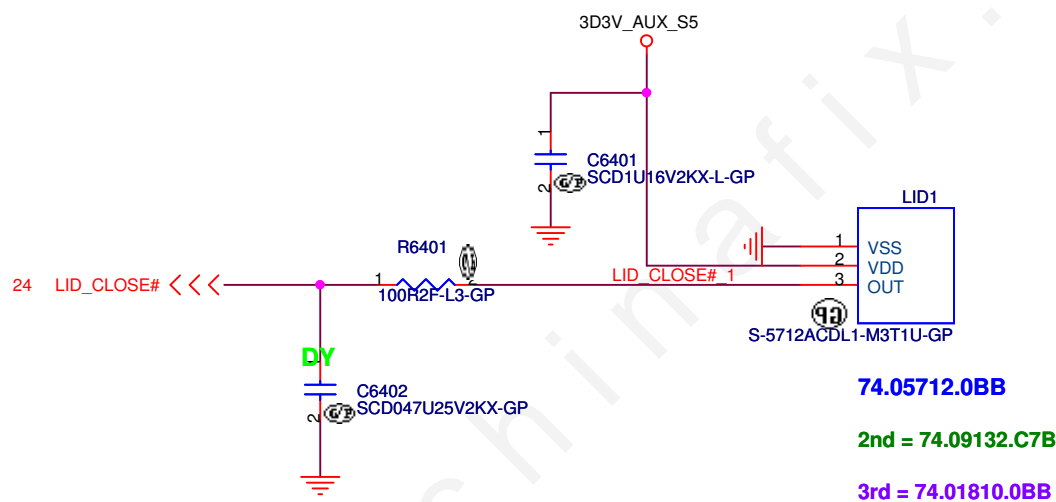
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Key Board/Touch Pad	
Size Custom Document Number Date: Tuesday, June 17, 2014	Rev Poseidon 860M Sheet 62 of 102



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<div>IO Board Connector</div>			
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

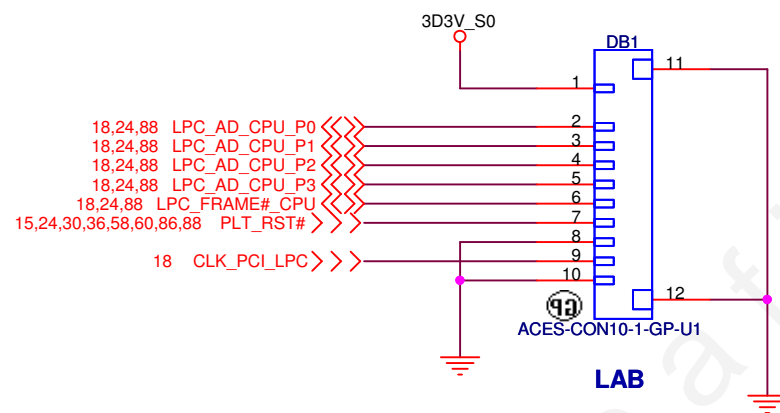
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
A4

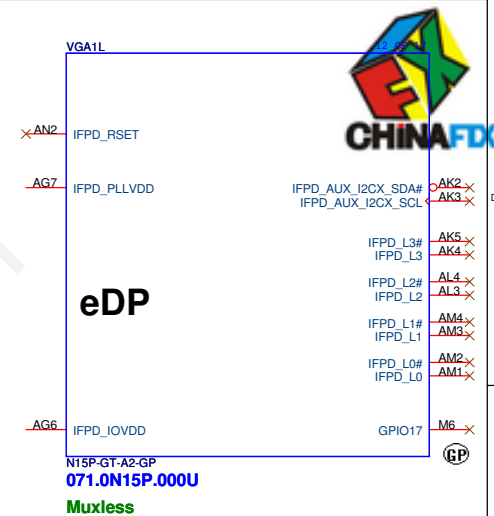
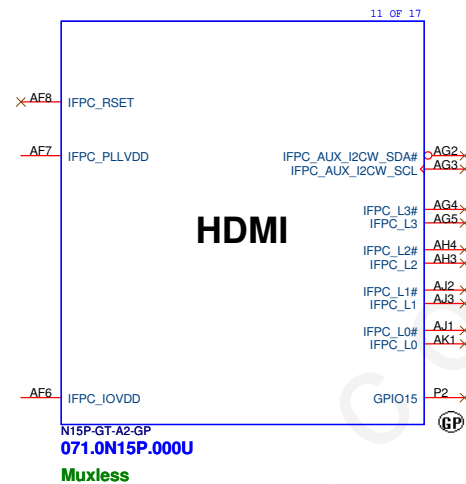
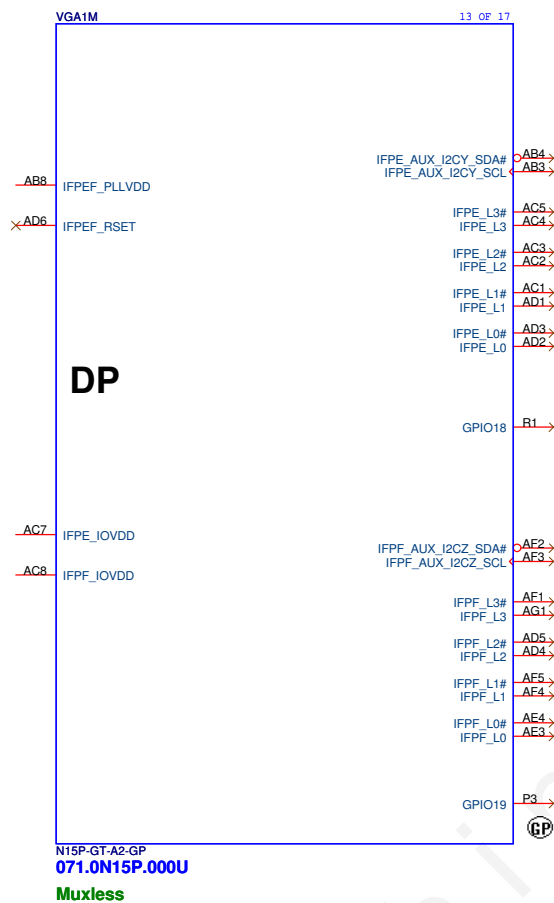
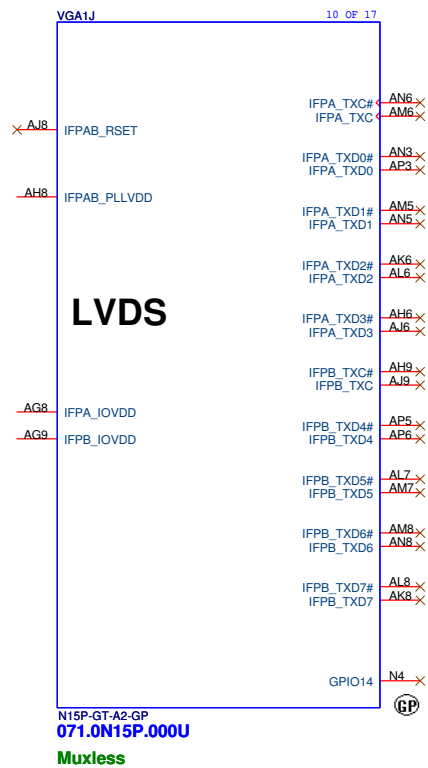
Document Number

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Title		
GPU (DIGITALOUT)		
Size A3	Document Number	Rev -1
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TABLE
GDDR5 VIDEO MEMORY

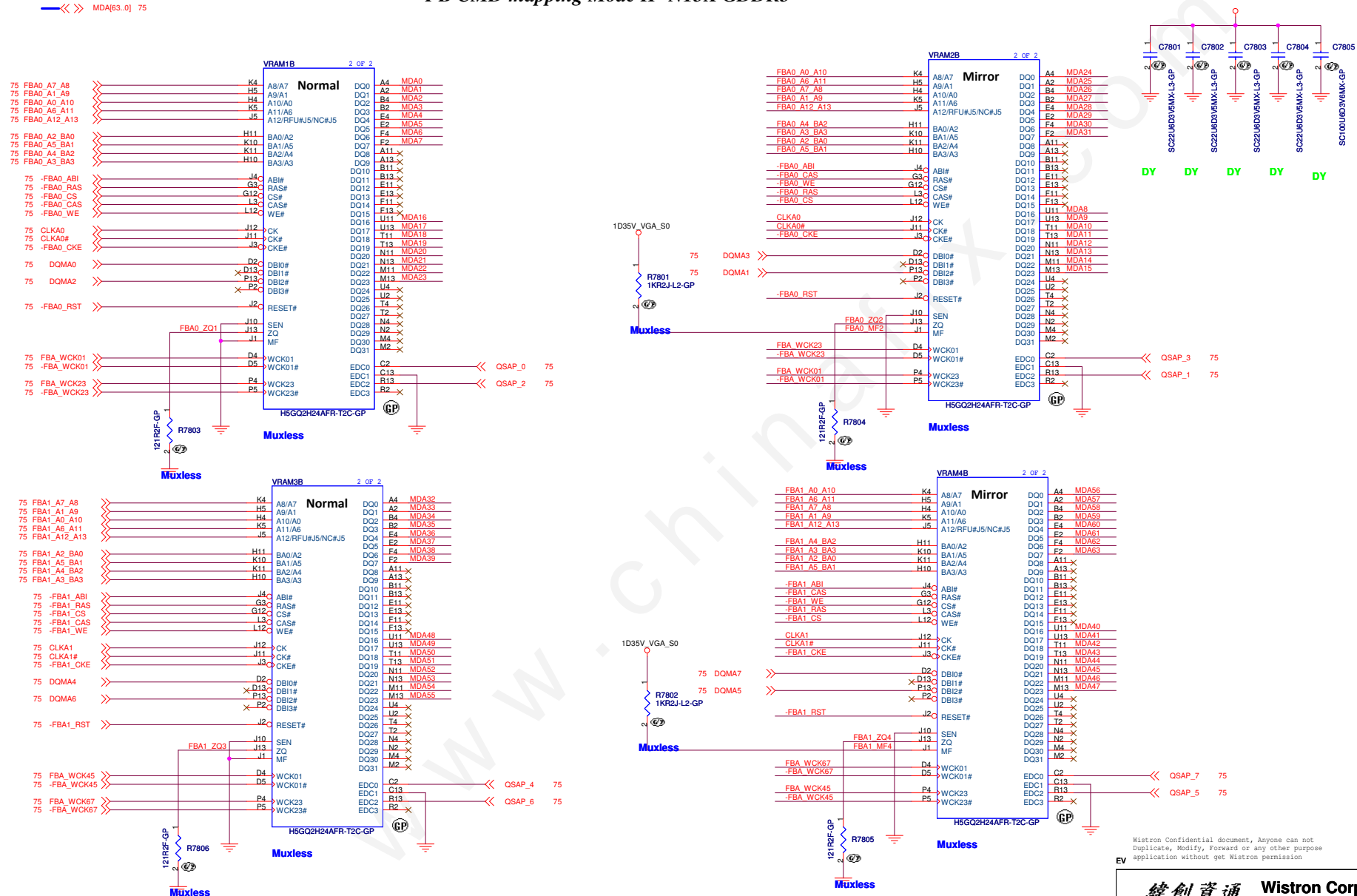
72.05224.A0U

72.20325.B0U

	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

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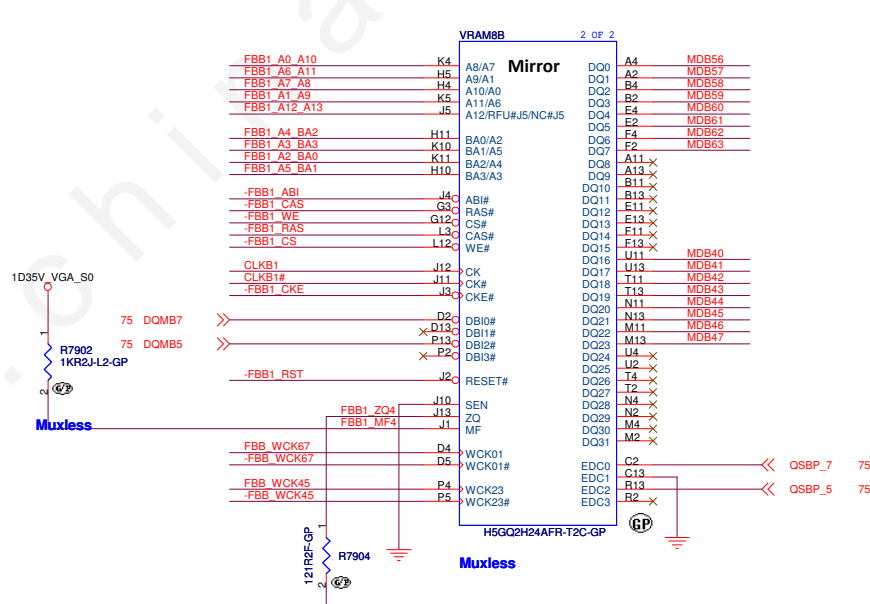
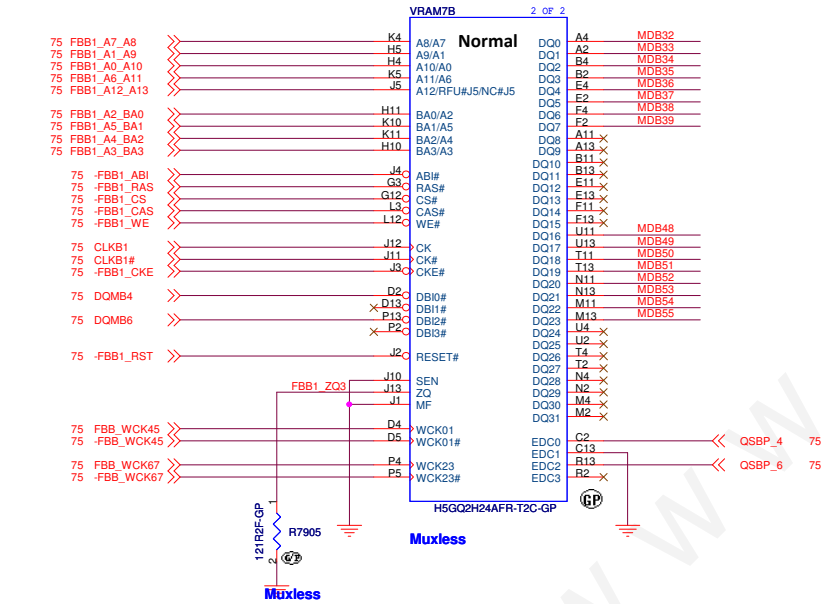
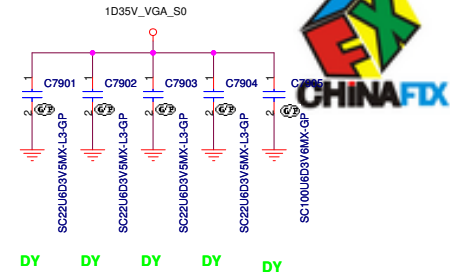
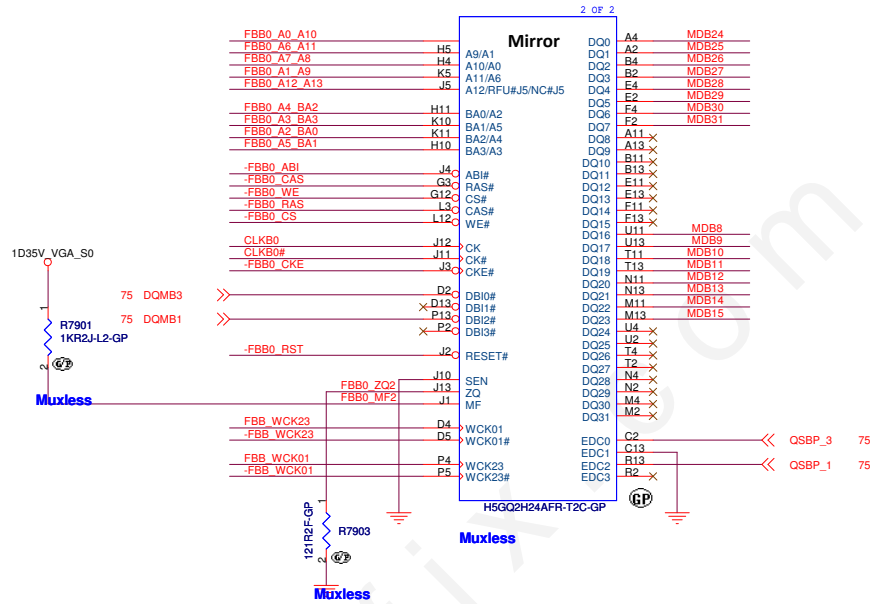
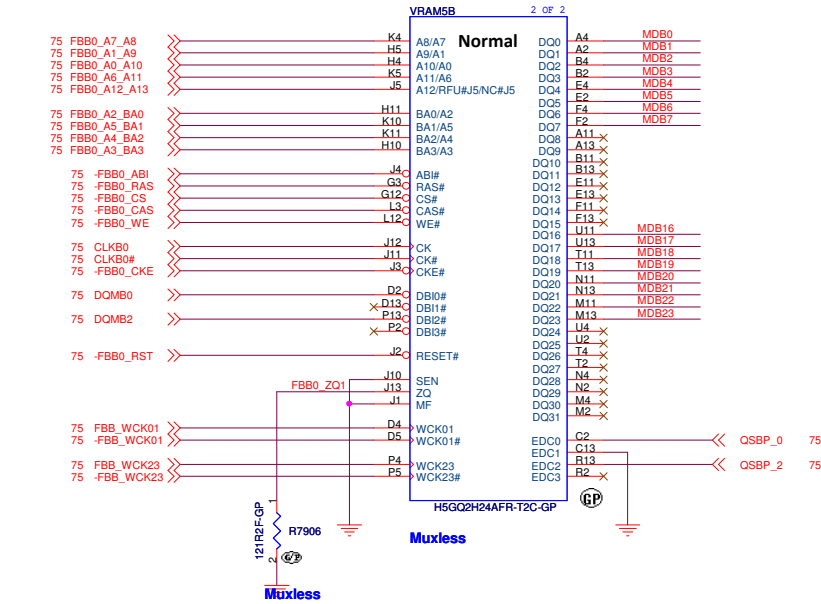
FB CMD mapping Mode H -N15X GDDR5



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Title	VRAM A
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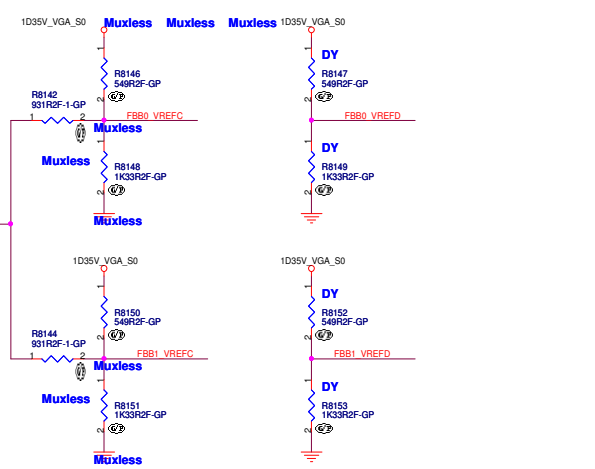
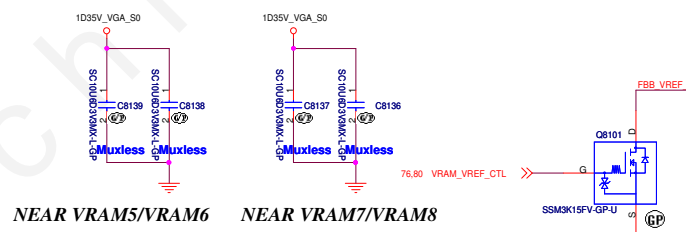
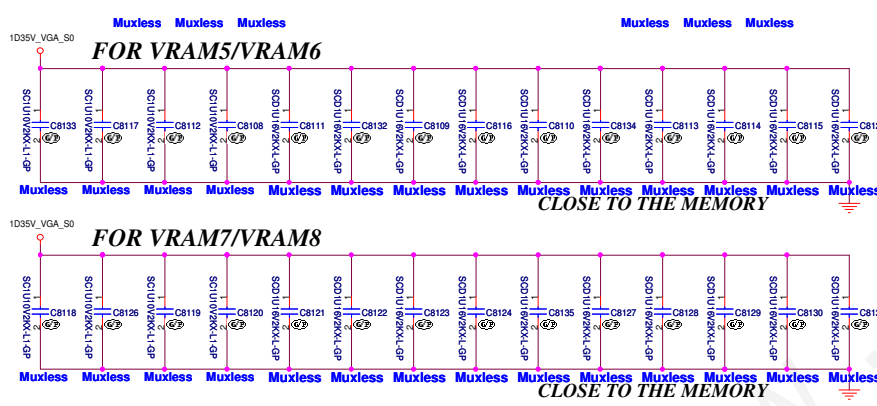
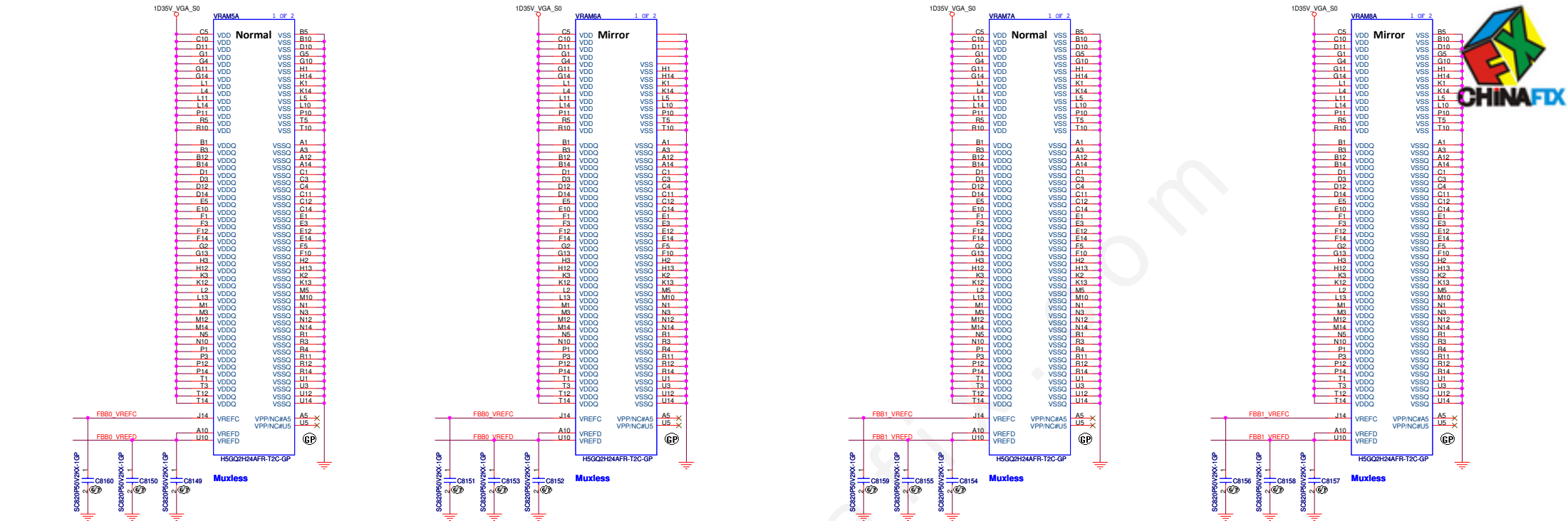
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Title: **VRAM B**

Size: **Custom** Document Number: **Poseidon 860M** Rev: **-1**

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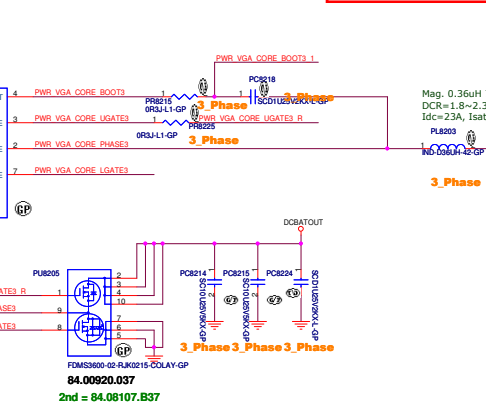
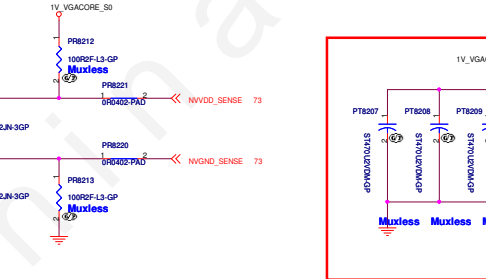
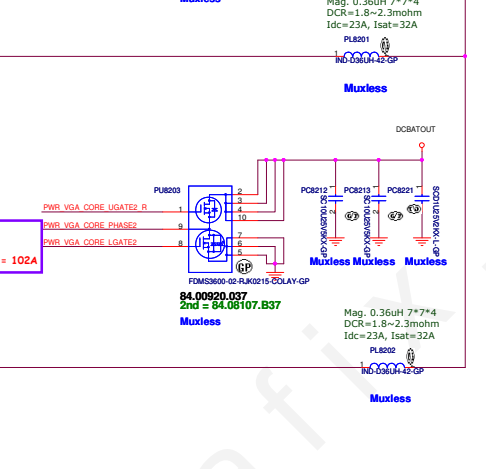
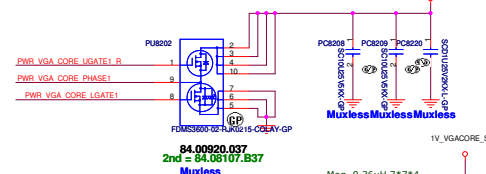
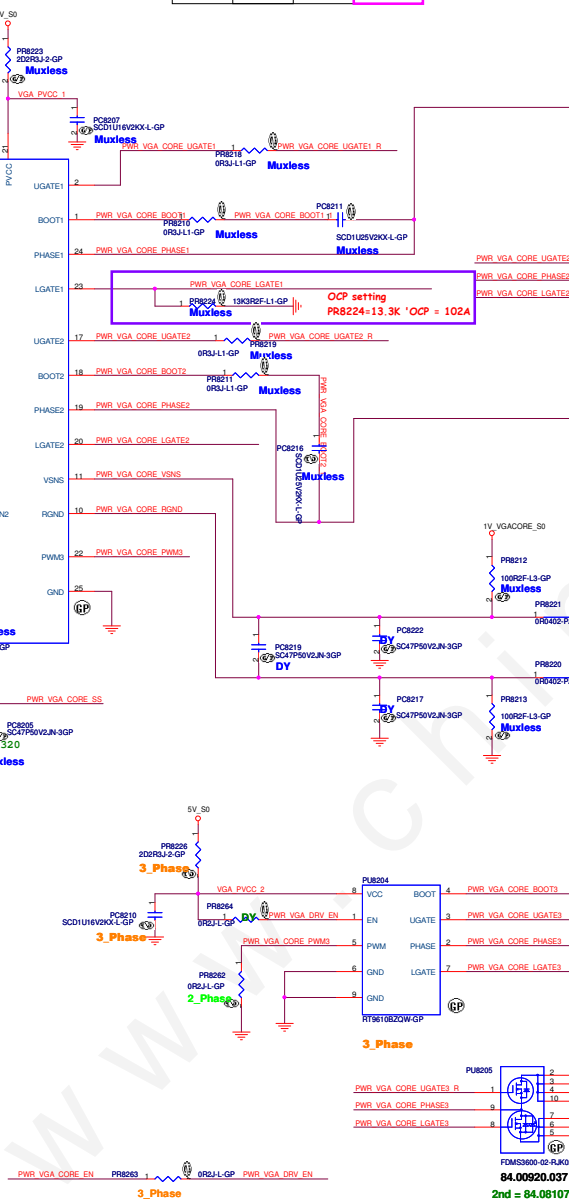
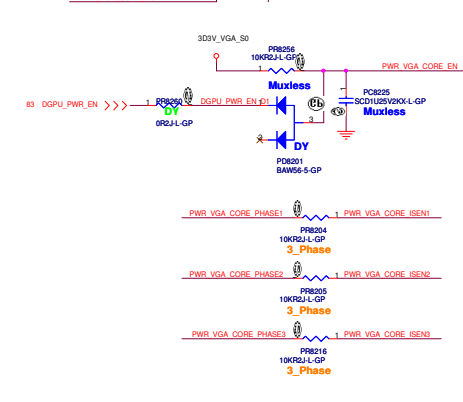
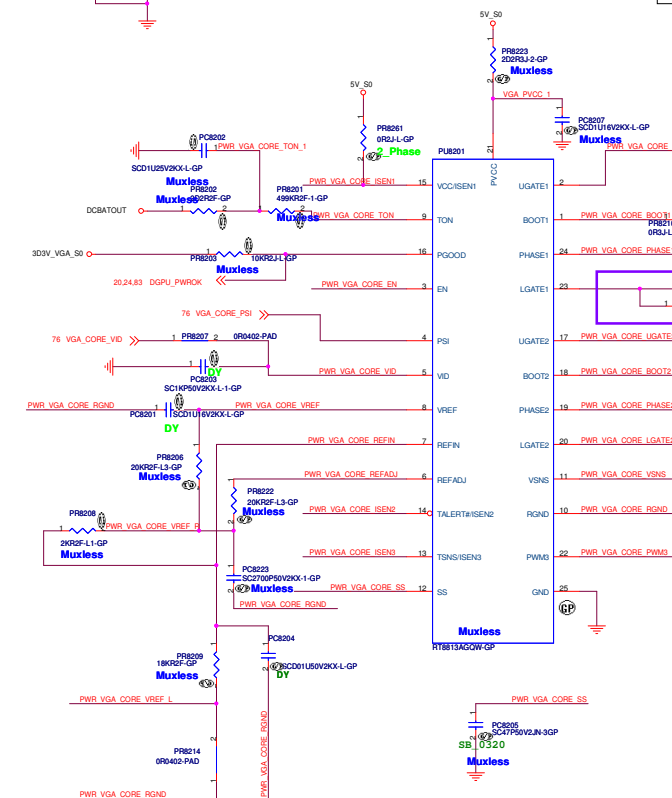
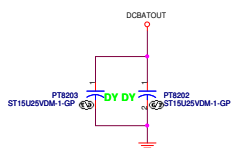
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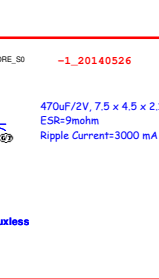
<http://vinafix.vn>

VGA : N15P 6X
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

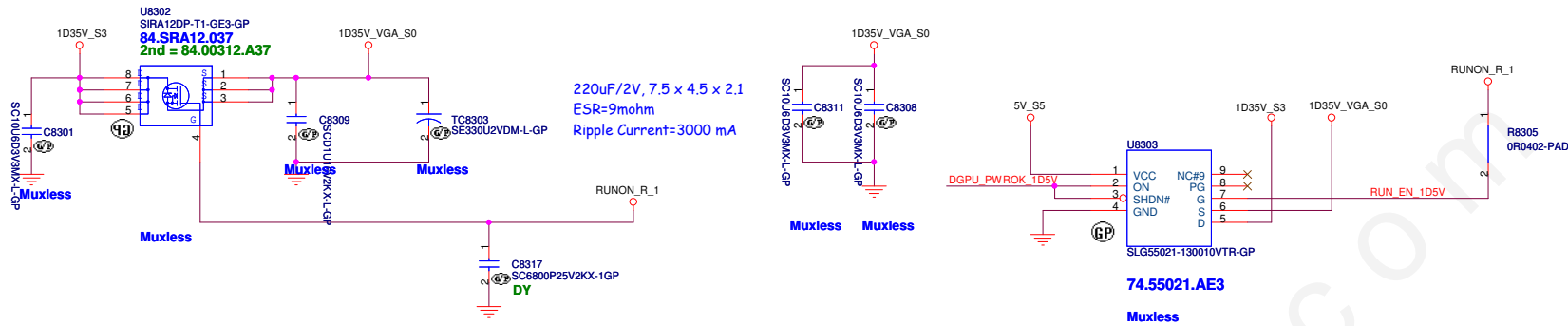
	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



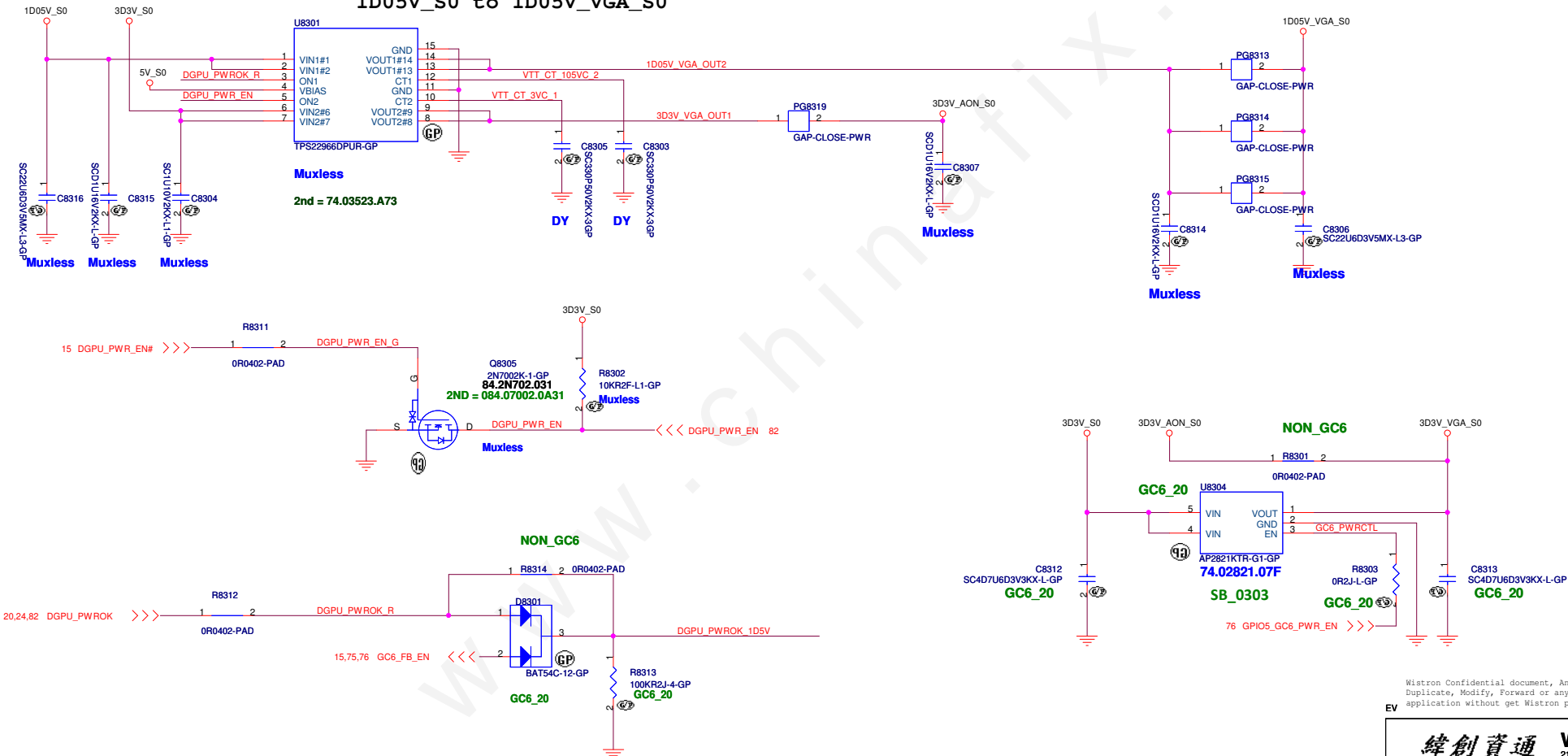
Dual NMOS
44.00916.037
2nd: 84.03660.037
PUB202/PUB203/PUB205



TPS22966 for VGA_1D35V(For VRAM GDDR5)



3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0

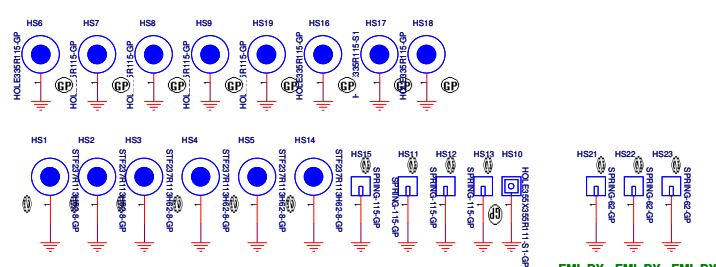


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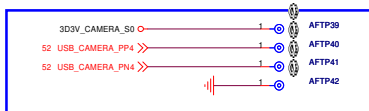
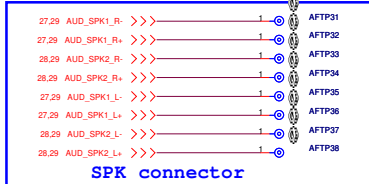
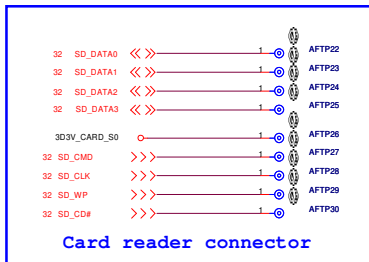
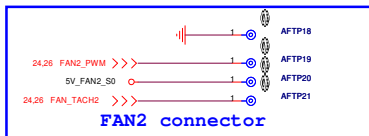
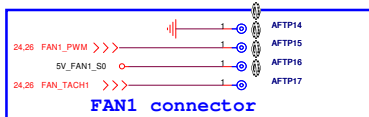
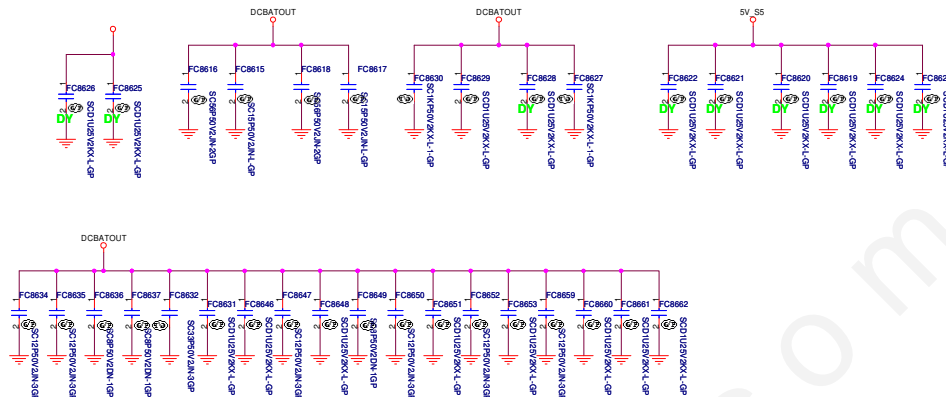
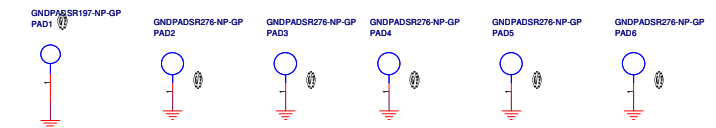
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DISCRETE VGA POWER		
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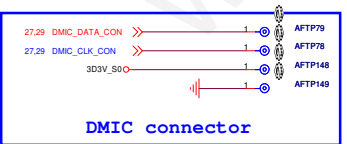
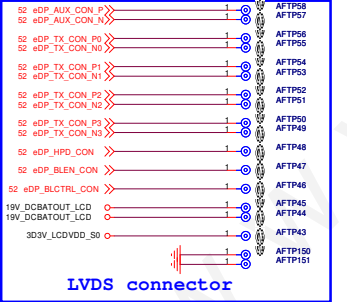
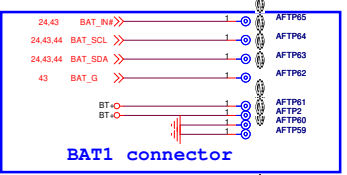
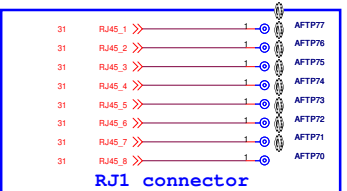
<http://vinafix.vn>



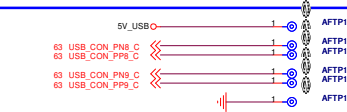
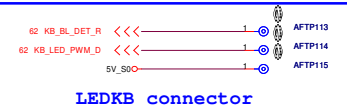
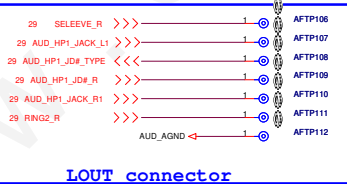
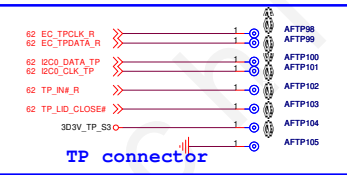
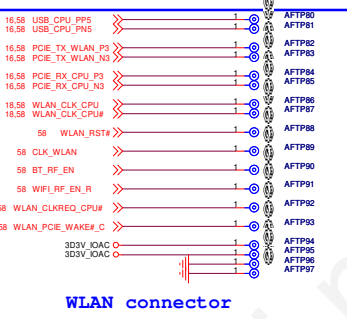
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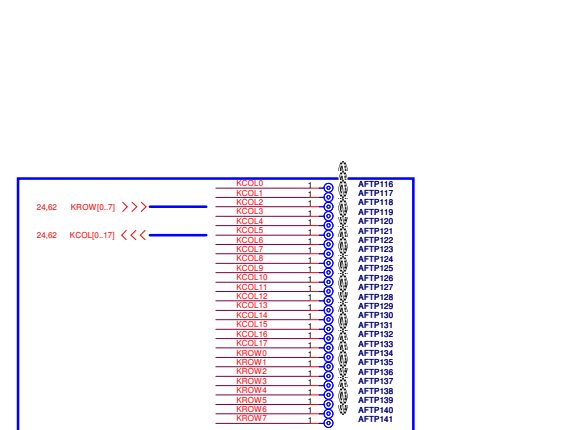
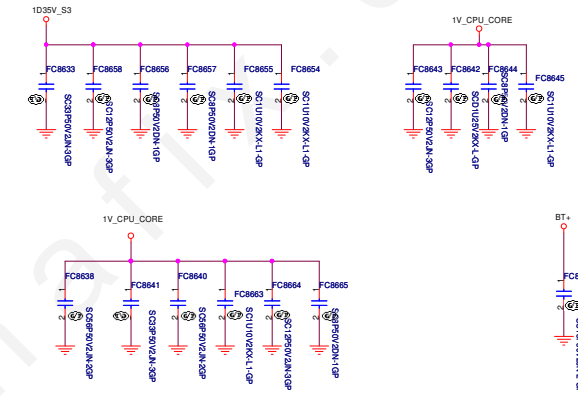
CCD connector



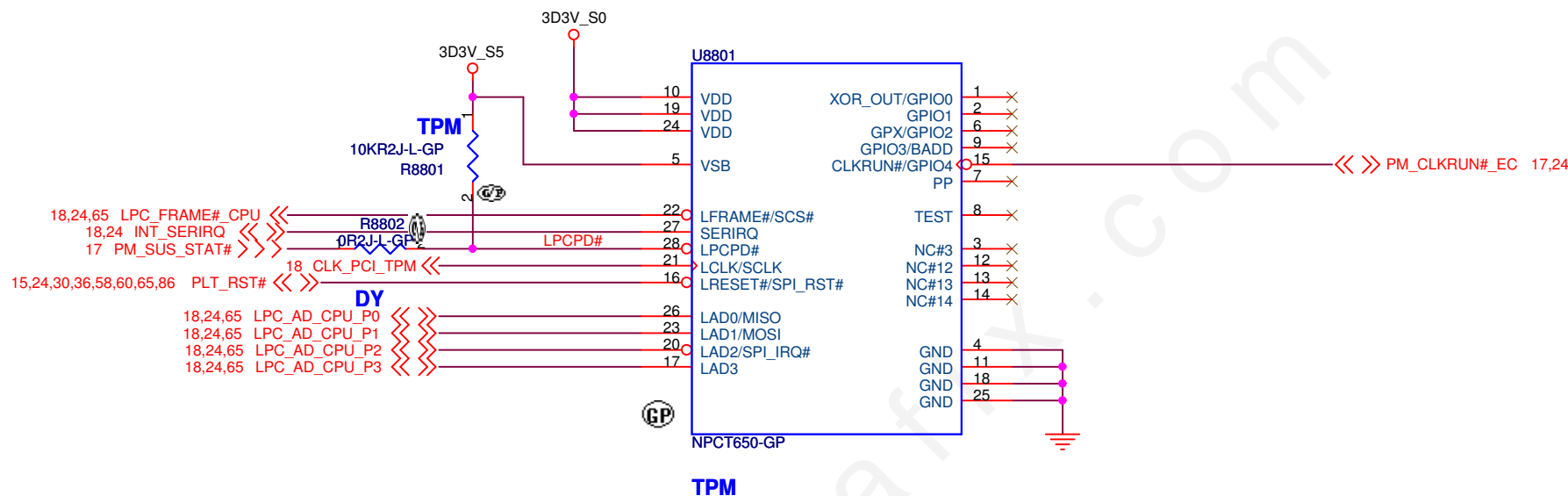
DMIC connector



I/O connector



KB connector



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Title **TPM (SLB655T)**

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EV

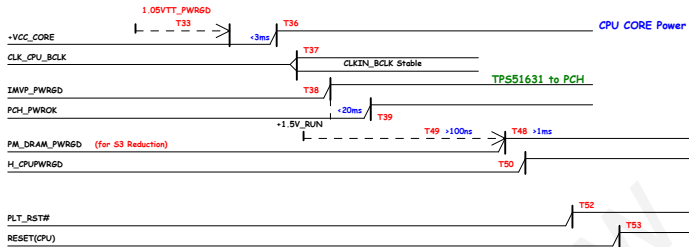
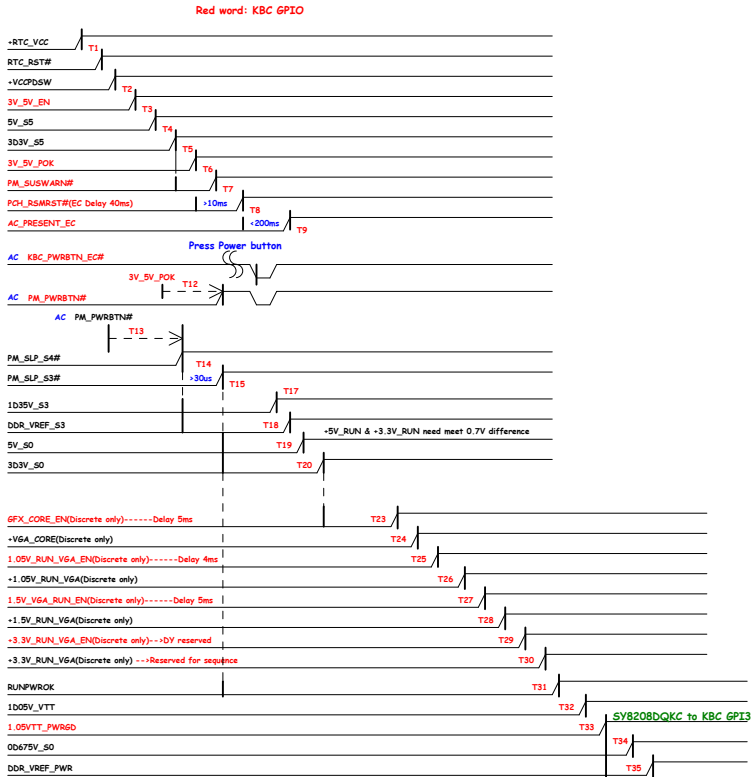
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Title			PCH_XDP	
Size A4	Document Number	Poseidon 860M		Rev -1
Date:	Tuesday, June 17, 2014	Sheet	96	of 102

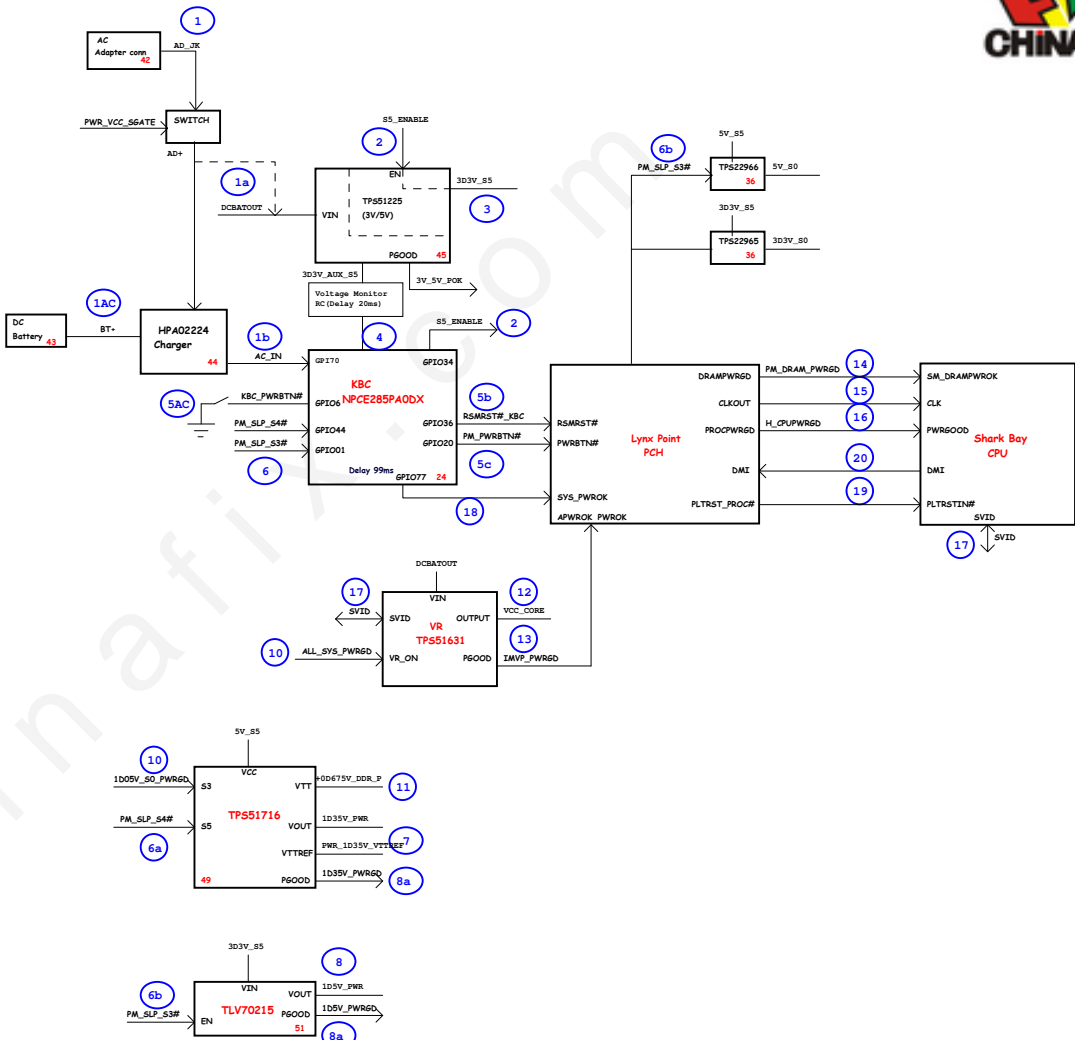
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1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	Open	NA	

<http://vinafix.vn>

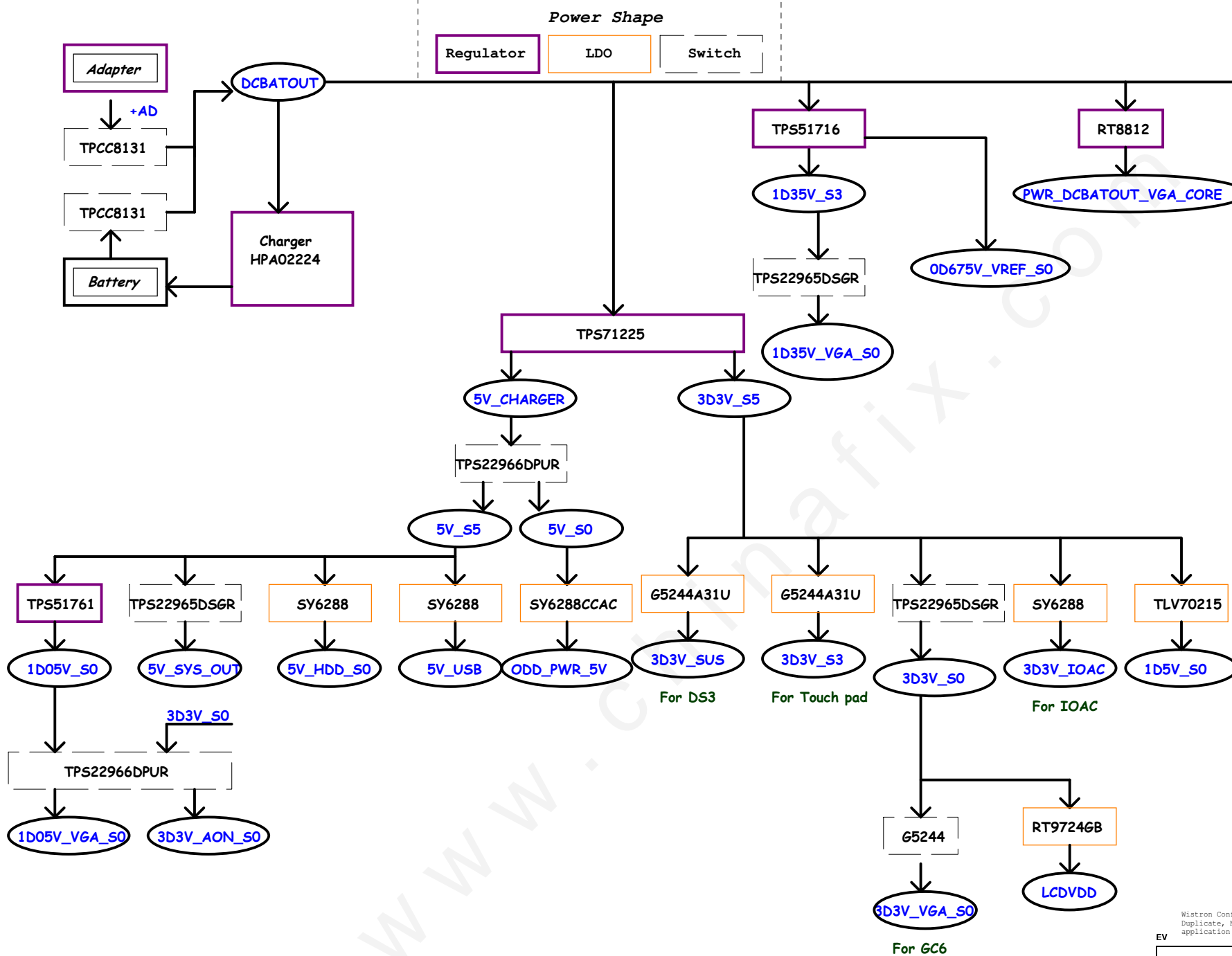
Intel-Power Up Sequence



SHARK BAY POWER UP SEQUENCE DIAGRAM

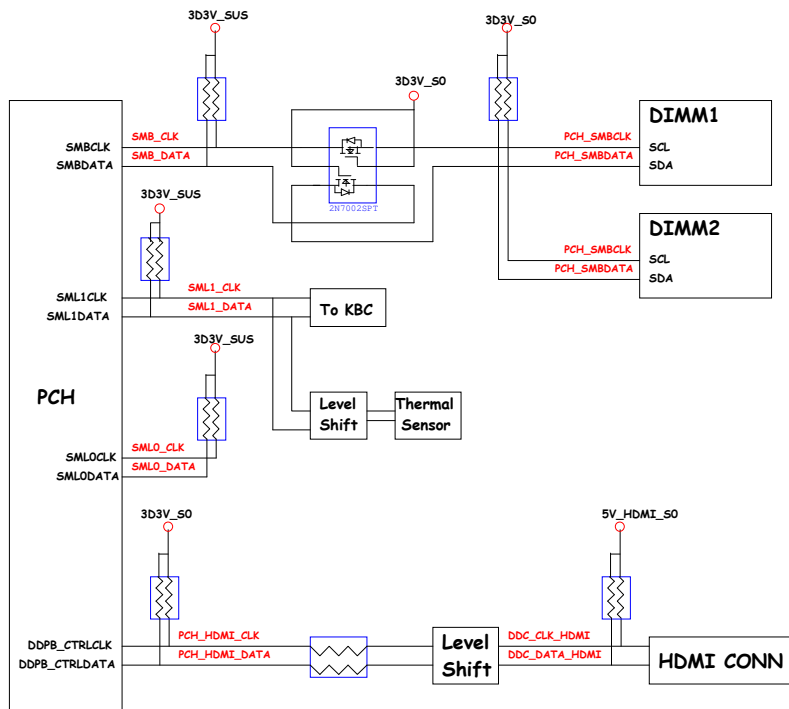


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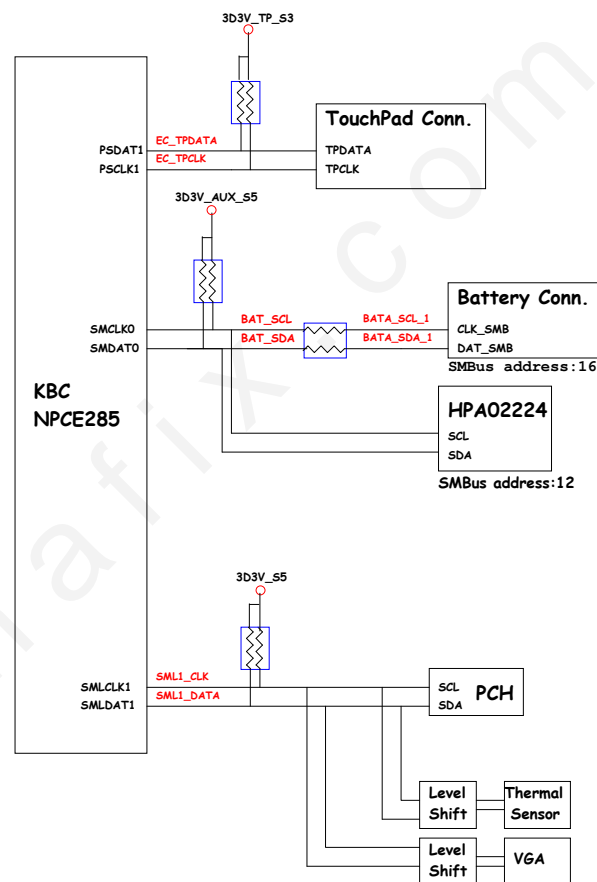


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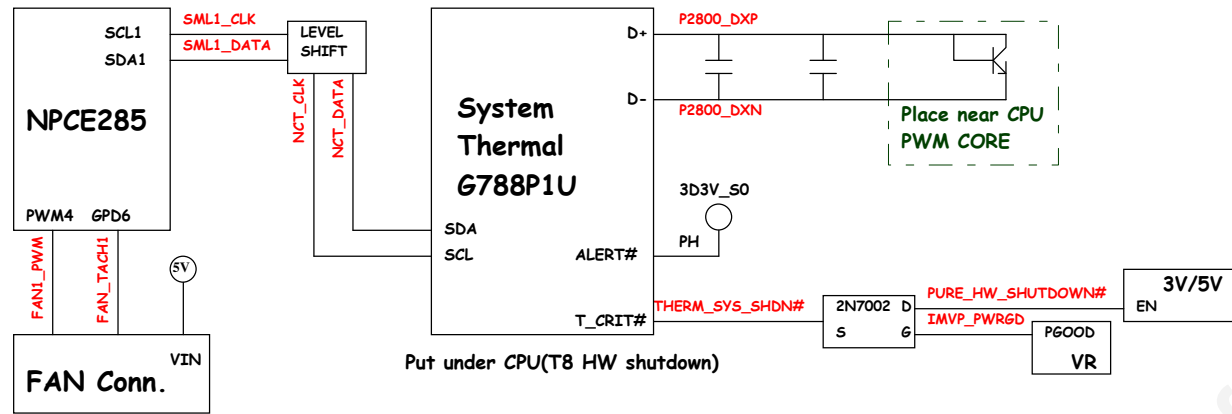
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

